1999

Plasma Enhanced Chemical Vapor Deposition of Silicon Nitride and Oxynitride Films Using Disilane as Silicon Source.

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PLASMA ENHANCED CHEMICAL VAPOR DEPOSITION OF SILICON NITRIDE AND OXYNITRIDE FILMS USING DISILANE AS SILICON SOURCE

A Dissertation

Submitted to the Graduate Faculty of the
Louisiana State University and
Agricultural and Mechanical College
in partial fulfillment of the
requirements for the degree of
Doctor of Philosophy

in

The Department of Electrical and Computer Engineering

by
Giridhar Nallapati
B.S., Mangalore University, India, 1990
M.S., Louisiana State University, 1992
May 1999

Dedicated to my parents

ACKNOWLEDGEMENTS

I would like, first, to express my deepest appreciation for the technical guidance and support given by my research advisor, Professor Pratul K. Ajmera. His thorough understanding of the many issues fundamental to semiconductor device physics and device operation, his attention to detail and basics that most often govern the behavior of even the most complex of problems will always be remembered. Needless to say, his belief in me made this work posible.

I would like to thank Drs. Kerry Dooley, Richard Kurtz, Gil Lee, Alexander Skavantzos and Ashok Srivastava for being a part of my dissertation committee. Special thanks to Dr. Rich Kurtz for being my minor professor.

I want to dedicate this work to my parents who, for inexplicable and sometimes unjustified reasons, always believed in me. These are two people I could always take for granted as though it is expected of me.

The two most special people I had a chance to associate myself with while at LSU are Dr. Juho Song, my fellow Ph. D. candidate and mentor (if that's possible), and Golden Hwaung, a person without whose help I would still be toiling trying to make my experimental setup work. Golden's practical knowledge of a broad range of things is a constant source of awe and inspiration. He is troubleshooter personified. I am thankful to Juho for giving me a direction both during and after my academic life.

There are countless other people whose names and faces pass through my mind as I ruminate about this period at LSU. People that I am lucky enough to know and get to know. Listing all those names would definitely make me miss this dissertation deadline. So, I would have to include all of them in saying that it was really a pleasure

knowing them and that aspect, as much as anything else, made this whole thing worthwhile.

Last, but not the least, I gratefully acknowledge the equipment grant, from the Louisiana Education Quality Support Fund granted by the Louisiana Board of Regents, that was used in acquiring the plasma CVD equipment used in this work.

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ABSTRACT

Process characterization details along with the electrical properties of plasma enhanced chemical vapor deposited silicon nitride and oxynitride films are reported, for the first time, using disilane as the silicon source.

Two regimes of deposition, namely excess-disilane regime and excess-ammonia regime, were observed for deposition of silicon nitride films using disilane, ammonia and helium. Films deposited under process conditions falling at the boundary of these two regimes had deposition rates that were mostly dependent on rf power and gas flow ratio resulting in highly repeatable film qualities.

Silicon nitride films deposited on Si wafers at 250 ^{0}C and post-metallization annealed in N_2 ambient at 420 ^{0}C exhibited fixed effective interface charge density of ~$3x10^{11}$ cm^{-2} and minimum interface state density of 2-3 x 10^{11} $cm^{-2}eV^{-1}$. The net bulk and interface charge density, charge trap density, interface trap density in the mid-bandgap region, and leakage current through the films were all lower for films that received a post-metallization anneal in both N_2 and forming gas ambients compared to the values for films annealed in either N_2 or forming gas ambients alone. All films exhibited higher instability due to hole trapping under negative gate bias stressing than due to electron trapping under positive gate bias stressing.

Silicon oxynitride films were deposited by introducing N_2O gas into the disilane/ammonia/helium gas system. Films deposited using higher N_2O flow rates exhibited higher net effective fixed interface charge densities. The charge trapping in the films decreased with increasing N_2O flow rates employed in deposition except at the highest N_2O flow rate investigated. In general, a turn-around behavior was observed in

the trend for several electrical properties of the oxynitride films with increasing N_2O flow rates. All the oxynitride films examined exhibited fewer occurrences of extrinsic breakdown compared to silicon nitride films, indicating reduction of pinhole density in the oxynitride films.

Reviewing the overall properties of these films, it was deduced that the silicon oxynitride films deposited using NH_3 to N_2O flow rate of 20 in the present system would be the most practical choice for their use as gate dielectric films in thin film transistor applications.

CHAPTER 1. INTRODUCTION

1.1 History of Nitride and Oxynitride Layer Usage in Semiconductor Industry

Dielectric silicon nitride films and their use in microelectronics technology were first mentioned as far back as 1964-65 when it was first discovered that these films have good masking properties with respect to diffusion of ions of different metals, especially sodium. A unique property of Si_3N_4 films, that of their capability to mask a semiconductor from the action of oxygen and water vapors at temperatures above 1000 ^{0}C, became known soon thereafter. This phenomenon resulted in the development of the local oxidation of silicon process (LOCOS) which is now widely used in microelectronics technology.

In MOS-LSI technology, it is recognized that the effectiveness of the final passivation layer to a large extent determines the ultimate reliability of the packaged device [Sinha et al., 1978]. The passivation layer protects sensitive areas of the device from outside contaminants, such as Na^+ ions and moisture, and also provides scratch protection to the top aluminum metallization layer. A potentially attractive material for this purpose is Si_3N_4 which provides an inert barrier to Na^+ ions and moisture. However, the use of Si_3N_4 had been restricted because of the high temperature (> 700 ^{0}C) required for chemical vapor deposition (CVD) of Si_3N_4 films and because of the built-in high tensile stress which limits the usable film thickness to approximately 200 nm [Sinha et al., 1978].

With the commercialization of plasma deposition technology in 1976 [Schwartz et al., 1979; Hasegawa 1978], Si_3N_4 films found more areas of application in integrated

circuit (IC) fabrication. The following advantages of *plasma* Si_3N_4 layers can be mentioned regarding applications to IC industry:

1) Low temperature (< 400 ^{0}C) deposition is possible. Hence, plasma Si_3N_4 can be deposited on the Al metallization layer.
2) A 1 μm thick film can be deposited on aluminum without cracks.
3) Plasma Si_3N_4 deposition has good step coverage on wafers with uneven surface topology.
4) Plasma process is compatible with Si-gate MOS device technology.
5) Plasma process offers a great degree of flexibility with respect to control of stress, film composition, density, and cracking resistance.

Because of the above factors, plasma enhanced CVD (PECVD) nitride films found their use as the final surface protective layers after the Al metallization step in IC industry. The PECVD nitride layers subsequently found various other applications such as diffusion mask [Hashimoto et al., 1986], passivation layer for semiconductor surfaces against electrical and chemical instabilities [Dell'Oca and Barry, 1972; Petroff et al., 1976], isolation and inter-layer insulation in multilayer metallizations [Milek 1972], encapsulant for III-V compound semiconductors [Helix et al., 1978], memory element in Metal/Nitride/Oxide/Semiconductor (MNOS) storage transistor [Uranvala et al., 1976; Goodman et al., 1970], oxidation mask [Turner and Connors, 1984] and as anti-reflection coating in GaAs and InP solar cells [Gupta et al., 1991].

Throughout this period, the potential of Si_3N_4 layers to replace SiO_2 in the electrically active regions of devices has been of some interest because of its higher dielectric constant and superior masking properties. However, due to the excellent bulk

and interface properties of SiO_2/Si structure, the Si_3N_4 layers have never really posed a threat as a viable replacement.

1.2 Impetus for Alternate Dielectrics and Dielectric Formation Processes

Present day complementary metal-oxide-silicon (CMOS) circuits with small (< 0.35 μm) gate dimensions and symmetric p- and n-channel devices with low threshold voltage values require ultra-thin gate oxides (4-6 nm equivalent of SiO_2 thickness) and dual poly-Si gates. The following are some of the problems associated with thermal SiO_2 in this thickness range:

1) In current CMOS technology, gate electrodes for p-channel field effect transistors are usually boron-implanted poly-silicon that require a high temperature dopant activation, during which boron atoms can diffuse through the thin SiO_2 dielectric layer degrading electrical properties of the oxide bulk as well as that of the SiO_2/Si interface [Ito et al., 1982; Sun et al., 1989].

2) High temperature oxidation can change the channel doping profile. On the other hand, low temperature oxidation of Si creates a large compressive stress and therefore a poor oxide-Si interface [Wolters and Zegers-van Dujinhoven, 1992].

3) A high tunneling current at low applied electric fields [Suzuki et al., 1983].

Initial suggestions for reducing B-atom diffusion through the oxide included the use of a dielectric with a higher diffusion barrier and/or a higher dielectric constant than that of SiO_2. The dielectric materials receiving the most attention in these regards are silicon nitride and silicon oxynitride.

Although Si_3N_4 has several desirable properties [Ito et al., 1982; Mori et al., 1991; Lo and Kwong, 1991], its major disadvantage lies in its poor electrical quality of

the Si_3N_4/Si interface for which values of interface state density, D_{it}, are typically in 10^{12} $cm^{-2}eV^{-1}$ range, or at least five times higher than that of the SiO_2/Si interface [Ma et al., 1993].

Si-O-N films formed by a nitrided oxide process have attracted the most sustained attention due to their potentially improved dielectric properties [Naiman et al., 1990; Joshi and Kwong, 1992; Gupta et al., 1987]. Some of these properties include improved breakdown strength, higher electrical permittivity, improved barrier to impurity diffusion, and superior resistance to plasma and radiation damage as compared to SiO_2. They also result in less charge trapping and higher endurance under electrical stress than oxides [Chen et al., 1985].

Different processes have been proposed for incorporating nitrogen in SiO_2. These include thermal nitridation in conventional furnaces or by rapid thermal processing (RTP), ion implantation, and plasma enhanced nitridation. Thermal nitridation in conventional furnaces does not seem useful for VLSI technology because of the high temperatures (1000-1200 ^{0}C) and long durations (> 1 h) that are required [Fazan et al., 1988]. In spite of this, a significant amount of research into alternate thin dielectric film fabrication still involves high temperature processing at one stage or other. Ion implantation produces a large density of defects, which can only be eliminated by moderately high temperature annealing. It thus seems that SiO_2 nitridation by rapid thermal cycles or in a plasma are the only viable techniques for VLSI circuits as they have a lower thermal budget. Plasma nitridation of thermal oxides remains a fairly unexplored territory with Fazan et al. providing the most details about this process with the authors concluding that it is possible to form nitrided layers with less electron trapping and higher endurance than oxides by properly adjusting process conditions.

The two types of nitroxides (or oxynitrides) that are currently attracting the most attention are: i) thermally nitrided oxides (NOX) and ii) reoxidized nitrided oxides (ROXNOX). The NOX dielectrics are composed primarily of SiO_2 with a small percentage (< 10%) of nitrogen at the Si/dielectric interface [Sodini and Krisch, 1992]. ROXNOX dielectrics involve an additional oxidation step at the end as this was found to help the reliability of the dielectric films through suppressed interface state generation under electrical stress [Krisch and Sodini, 1994]. Typical process sequences for the growth of ~11 nm thick thermal oxide, NOX, and ROXNOX at two different temperatures (850 ^{0}C, 950 ^{0}C) are given in Table 1.1 [Krisch and Sodini, 1994]. The growth sequence at 950 ^{0}C was performed at pressures one order lower than the process at 850 ^{0}C.

As mentioned earlier, most of the current research into future generation dielectrics still involves high temperature processing at some stage, be it the stage of thermal oxide growth at > 850 ^{0}C temperature or the later processing of thermal oxides for nitrogen incorporation or the reoxidization of the nitrided oxides. Recently, a low thermal budget process for the deposition of silicon oxynitride layers and stacked O-N-O dielectrics has been proposed where the films are prepared by combining remote plasma-enhanced chemical vapor deposition (RPECVD) at 300 ^{0}C and rapid thermal annealing (RTA) at 900 ^{0}C [Ma and Lucovsky, 1994].

Another device structure with need for alternate gate dielectric and dielectric formation process is metal-insulator-semiconductor thin film transistor (TFT). TFTs are used as switches that control voltages on individual pixels in an active matrix liquid crystal display (AMLCD). The cross-section of a typical amorphous silicon TFT structure is shown in Fig. 1.1. The TFT fabrication process must be conducted at 450 ^{0}C

Table 1.1. Typical process conditions for furnace dielectrics [Krisch and Sodini, 1994].

Temperature	Dielectric	Gas	Time
850 °C	OXIDE-LT	O_2	55 min
	NOX-LT	O_2 NH_3	55 min 1 h
	ROXNOX-LT	O_2 NH_3 O_2	55 min 1h 3h
950 °C	OXIDE	O_2	55 min
	NOX-LP	O_2 NH_3	55 min 1 h
	ROXNOX-LP	O_2 NH_3 O_2	55 min 1 h 3 h

LT – Low Temperature
LP – Low Pressure

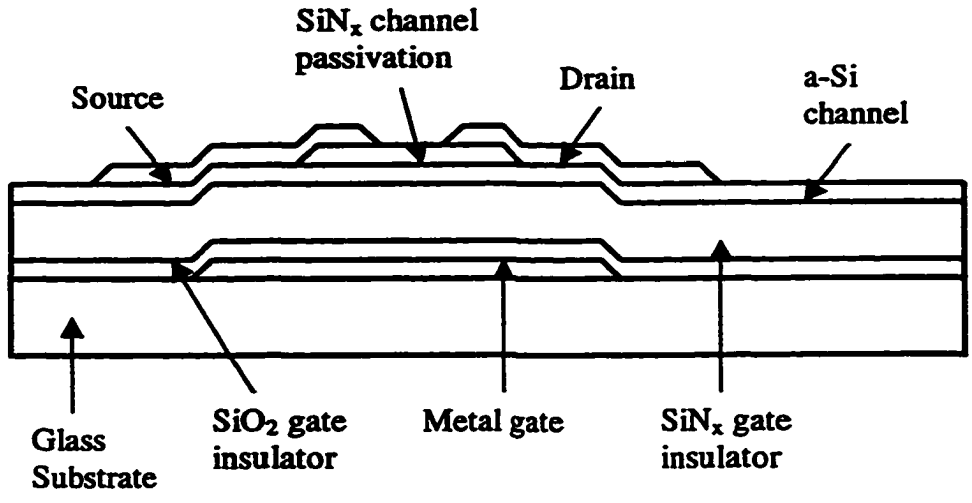


Fig. 1.1. Typical cross-section of an inverted-type amorphous-Si thin film transistor (TFT). A stacked SiN_x/SiO_2 layer is used as the gate dielectric in this transistor.

or lower in order to be able to use low cost glass as the substrate material. This creates the need for a low temperature (< 400 °C) dielectric deposition process with the resultant films having excellent thickness uniformity, electrical characteristics and step coverage.

1.3 Plasma Enhanced Chemical Vapor Deposition (PECVD) and Plasma Chemistry

Plasmas are gaseous media that contain enough ions and electrons to be electrically conductive [Thornton 1983]. Energy is introduced into the plasma by the acceleration of electrons in a dc, rf or microwave field. These electrons, through elastic and inelastic collisions, then fragment, excite and/or ionize source molecules so as to make them more chemically active or "activate" them. This is schematically expressed in the form of an energy flow diagram in Fig. 1.2. In most cases, the processing plasma is a "weakly ionized" plasma such that there are many more neutral particles than ions in the gas phase (ratio of 10^7 to 10^4 : 1), the average ion energy is low (few meV), the electron density is low (< 10^{10} cm^{-3}) and the average electron energy is 1 to 10 eV [Auciello 1990]. In PECVD, the plasma-activated species, through the formation of gas-phase precursors and their subsequent transport to the substrate, allow the deposition of amorphous material and make it possible to decrease the temperature needed to decompose a chemical vapor species on the substrate surface [Veprek 1985]. There are also instances where no gas-phase precursors are formed and film deposition is accomplished by reactions between the surface adsorbed species. In either case, surface diffusion and rearrangement of reactive species are dependent on the substrate temperature which plays a major role in determining the film composition, bonding configuration in the films and the film density.

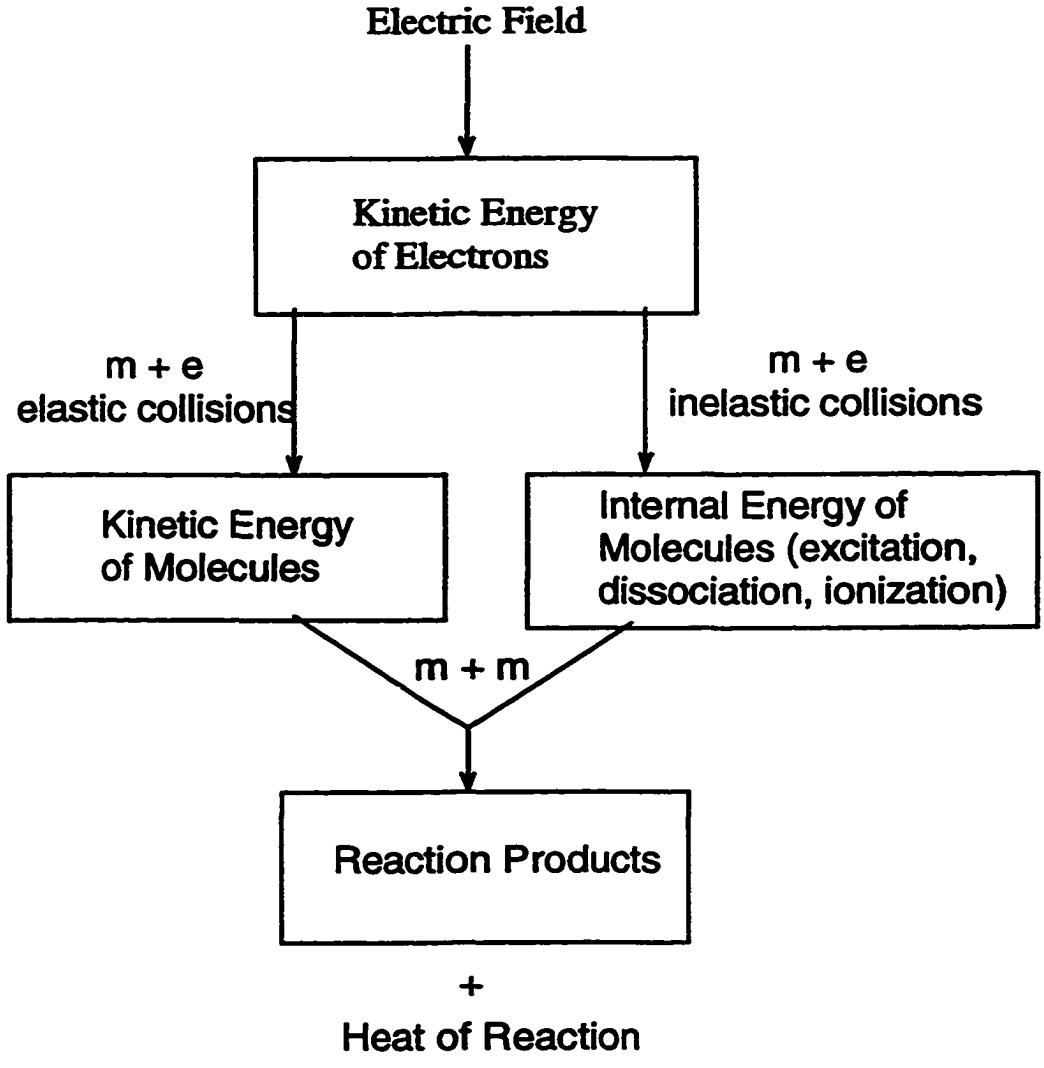


Fig. 1.2. Energy flow diagram in plasma. Symbols m and e indicate molecule and electron respectively [Sugano 1985].

Although Si_xN_y thin film deposition by PECVD had been studied for a long time, little was known about the plasma chemistry of the deposition process until Smith et al. reported, for the first time, an analysis of the plasma chemistry of Si_xN_y PECVD from SiH_4/NH_3 [Smith et al., 1990] and SiH_4/N_2 [Smith et al., 1990] gas mixtures. The authors used line-of-sight sampling from the film deposition plane into a triple-quadrupole mass spectrometer (TQMS), which can resolve compositional ambiguities at a given mass number by utilizing collision-assisted secondary cracking. The results for the SiH_4-NH_3 deposition system will be detailed first.

1.3.1 The SiH_4-NH_3 System

From mass spectrometric analysis carried out by Smith et al., disilane (Si_2H_6) and the aminosilanes ($SiH_{4-n}(NH_2)_n$) were found to be the principal products of an ammonia-silane plasma [Smith et al., 1990]. Rf power was the main determinant of the disilane to aminosilane product ratio. At low rf power values, owing to the fact that ammonia requires more electron energy to be activated than does silane, the reaction towards formation of disilane is favored, with much less tri- and tetra-aminosilane formation. Disilane results from silane radicals reacting with each other and with silane. So, at low rf powers, NH_3 behaves more like an inert diluent. At higher powers and with sufficient excess of NH_3, the reactions resulting in formation of aminosilanes take over, consuming most of silane and thus preventing the formation of disilane. Under these conditions, termed as the aminosilane regime, the following reactions are predominant:

$$SiH_4 + e^- \longrightarrow SiH_3 + H + e^-$$

$$SiH_3 + NH_2 \longrightarrow SiH_2(NH_2) + H\,.$$

Since radical-radical reactions typically have no activation energy and occur at collision rates, the amination of silane radicals is expected to proceed until the silane becomes saturated to $Si(NH_2)_4$. The overall reaction, then, would be:

$$SiH_4 + 4NH_3 \longrightarrow Si(NH_2)_4 + 4H_2 .$$

In the above sequence of reactions, NH_2 is used as the active state of ammonia in the plasma just to illustrate the successive amino reaction, as direct proof of its existence is not available. Some of the possible candidates for this reaction include: NH_3^*, NH_2, NH, NH_2^-. Also, the eventual product, $Si(NH_2)_4$, might be unstable in the plasma environment and lose its first NH_2 to make the $Si(NH_2)_3$ radical dominant. The above results are evident in Fig. 1.3 which shows the dependence of several mass peaks and the deposition rate on the rf power.

Based on the observation that increasing substrate temperature causes film densification and causes a decrease in hydrogen and excess nitrogen concentrations in the films, a process by which $Si(NH_2)_3$ is converted to SiN_xH_y at the surface has been proposed (see Fig. 1.4) [Smith et al., 1990]. According to this model, the film densification occurs in a chemical "condensation zone" which extends below the surface. The condensation mechanism proceeds as follows: A $Si(NH_2)_3$ radical adsorbs on a nitrogen site, most likely one from which hydrogen has desorbed to form NH_3. Some $Si(NH_2)_4$ will likely adsorb as well, with the first NH_2 group being released in the process. Amino (NH_2) groups from neighboring $Si(NH_2)_3$ adsorbed molecules on the surface react with each other to evolve NH_3 as shown, leaving a Si and a N dangling bond which combine to develop the Si-N network. Further beneath the surface, the material can be thought of as a Si-N network with some of the bonds not yet formed, the

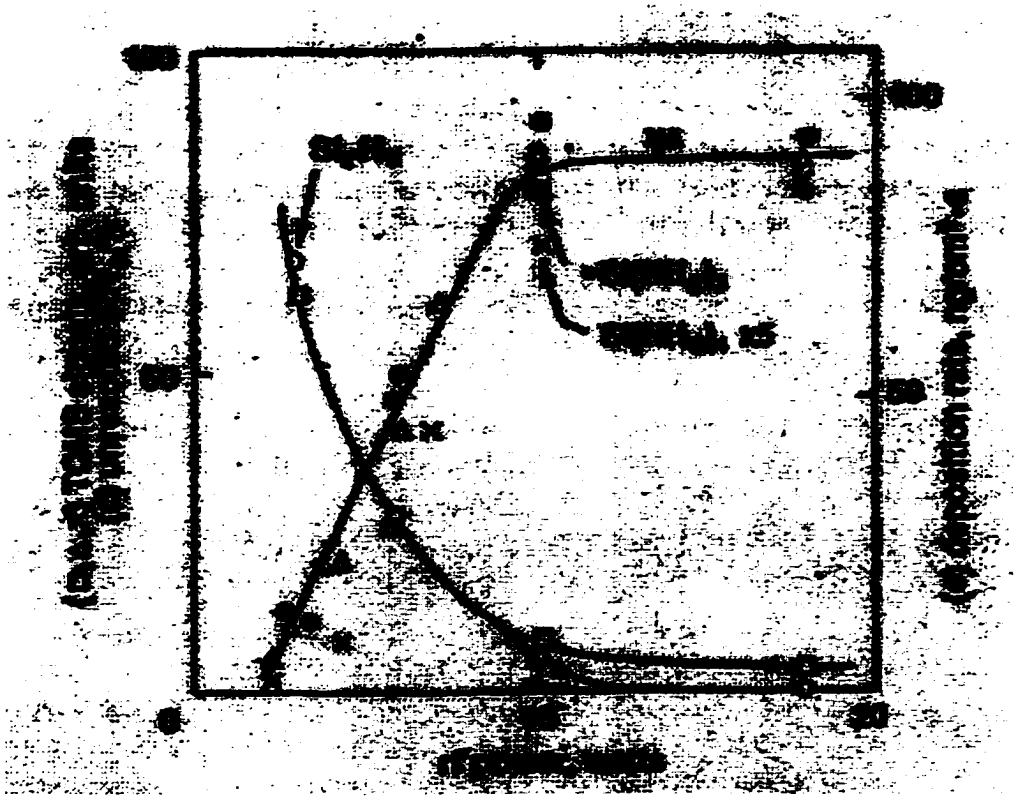


Fig. 1.3. Plasma composition and film mass deposition rate vs rf power, while operating at 160 Pa process pressure, 45 sccm NH_3, 1.8 sccm SiH_4, and 290 °C deposition temperature [Smith et al., 1990].[1]

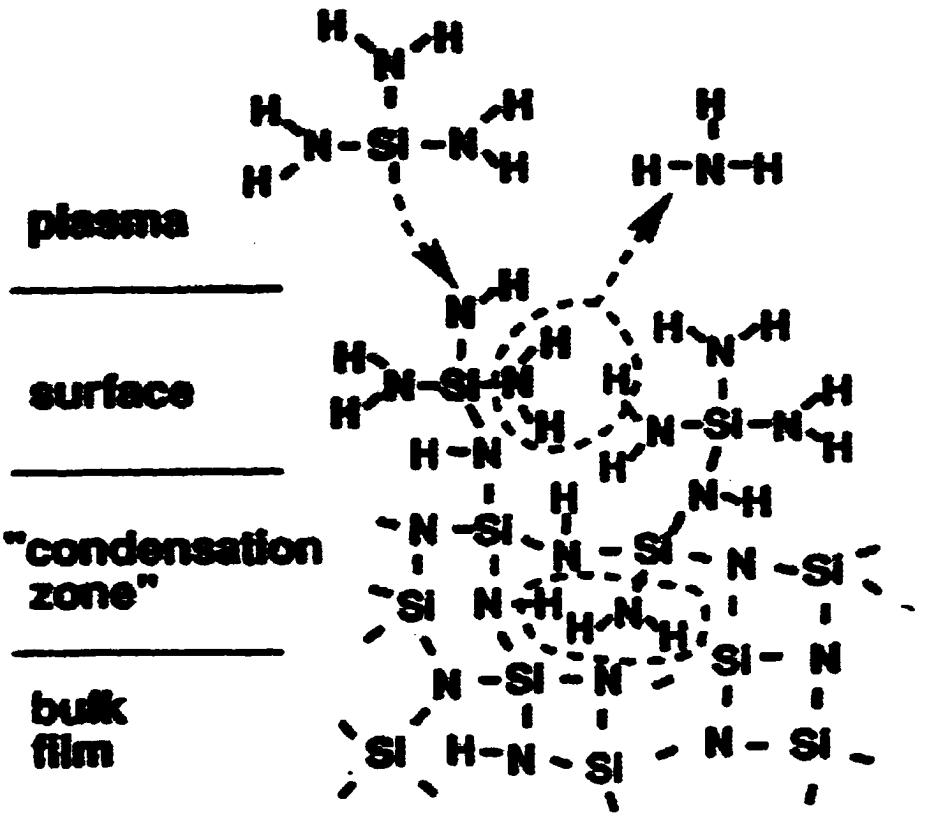


Fig. 1.4. Cross-sectional structure model of the condensation of adsorbed $Si(NH_2)_3$ toward a Si-N network with the evolution of NH_3 [Smith et al., 1990].[2]

[2] Reprinted with permission from Electrochemical Society, Inc.

Si halves being attached to excess NH_2 and the N halves to excess H (Fig. 1.4). Condensation proceeds as long as these excess species can reach each other and combine to release NH_3.

So, the overall chemistry of PECVD deposition of silicon nitride from NH_3 and SiH_4 sources under amino-saturated conditions may be written in a balanced equation form as a gas phase precursor-forming reaction,

$$SiH_4 + 4NH_3 \xrightarrow{\text{plasma}} Si(NH_2)_4 + 4H_2$$

followed by a surface condensation reaction,

$$3Si(NH_2)_4 \xrightarrow{\text{heat}} Si_3N_4 + 8NH_3\uparrow .$$

Also, silicon nitride films deposited in the aminosilane regime have been found to be N-rich. The films deposited otherwise are either stoichiometric or Si-rich. Hence, film composition is found to be predominantly dependent on the rf power and silane flow rate ratio. This behavior is expressed in Fig. 1.5 which shows a qualitative plot of the deposition rate of nitride films as a function of rf power and silane flow rate. This behavior will be discussed further in section 2.3.

1.3.2 The SiH_4-N_2 System

In the SiH_4-N_2 system, at low values of rf power, the plasma products are disilane and hydrogen [Smith et al., 1990]. Similar to the SiH_4-NH_3 system, the disilane can be eliminated by operating at sufficiently high rf powers and/or low silane flow rates if an excess of nitrogen atoms is present. Conversely, when there is insufficient power to activate the N_2, or when there is too much silane to be consumed by the activated N_2, then the silane radicals react with each other to form disilane.

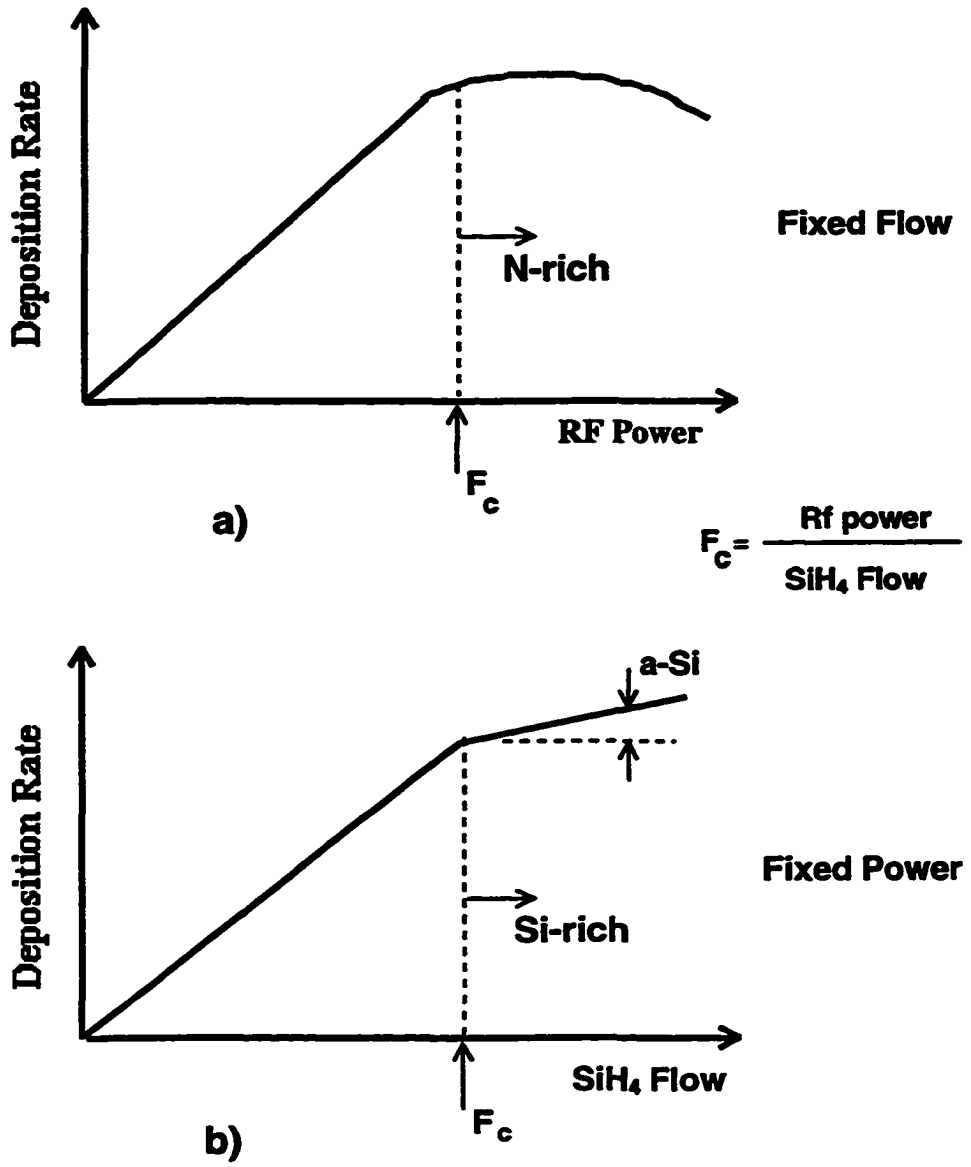


Fig. 1.5. Deposition rate of silicon nitride films as a function of a) rf power at fixed silane flow and b) silane flow at fixed rf power. The N-rich and Si-rich regimes are indicated by arrows. The critical ratio of rf power and silane flow rate that demarcates these two regimes is indicated by F_c.

But, unlike the SiH_4-NH_3 process where aminosilanes are the precursor species, the N_2 process has no Si-N species in the plasma and the silicon nitride deposition proceeds by direct reaction of SiH_n radicals and activated nitrogen at the substrate surface.

1.4 Film Properties : A Brief Review

Due to the variety of process parameters available in a PECVD process, a wide range of physical, chemical, mechanical, optical and electrical properties have been reported in the literature for silicon nitride and oxynitride films. In fact, this very aspect of PECVD is responsible for its employment in deposition of various kinds of films with a wide range of properties for a variety of applications in semiconductor industry and elsewhere. Due to the complexity and non-equilibrium nature of PECVD process and also its dependence on the reactor geometry, reported results are not always consistent. Despite this, there exist certain definite trends of film properties with respect to different process variables and these are briefly reviewed below.

1.4.1 Silicon Nitride Films

1.4.1.1 Thickness/Deposition Rate/Density

Higher deposition temperatures result in denser films, thereby causing lower deposition rates [Sinha et al., 1978]. The deposition rate increases with chamber pressure and with SiH_4-to-NH_3 ratio [Kuwano 1969]. Low deposition rates usually yield denser films and slower etch rates [Claassen et al., 1983]. The density of Si_xN_y films deposited in SiH_4/NH_3 system shows a broad peak for SiH_4/NH_3 ratio between 0.6 and 0.8 [Gupta et al., 1991]. The density is unaffected by total pressure and increases with substrate temperature, T_S [Blauw 1984].

1.4.1.2 Composition

The composition of PECVD Si_xN_y layers is determined by the [Si]/[N] atomic ratio, the [Si-H]/[N-H] bond ratio in the film and the total amount of hydrogen incorporated in the film [Claassen et al., 1983]. The films are Si-rich for [Si]/[N] ratios in the film greater than 0.75 and N-rich for ratios lower than 0.75. The SiH_4/NH_3 flow ratio and rf power together influence the [Si]/[N] ratio in the films. The hydrogen concentration in the films is strongly dependent on the substrate temperature and is reported to range from 4 to 39% atomic [Chow et al., 1982]. There is an appreciable decrease (almost exponential) in H-content with increasing T_s.

1.4.1.3 Etch rate

The effect of various process variables on the etch rate are outlined below:

1) The etch rate in buffer HF (BHF) is found to be very sensitive to the H-content [Chow et al., 1982]. As the H-content decreases with increasing T_s, the etch rate decreases appreciably. A universal correlation between the etch rate and H-content was demonstrated by Chow et al [1982].

2) The H-content decreases after annealing at higher temperatures (around 500-600 ^{0}C) and hence the etch rate also decreases after annealing [Gupta et al., 1991].

3) The etch rate in BHF is a function of the [Si]/[N] atomic ratio in the film. It increases as the [Si]/[N] atomic ratio in the film decreases [Claassen et al., 1983].

1.4.1.4 Electrical Properties:

Electrical properties include the properties of Si_xN_y/Si interface, charge content in the films, charge trapping, dielectric constant, electrical resistivity, the mechanism of

carrier conduction, and the breakdown voltage. These properties are deduced from capacitance-voltage (C-V) and current-voltage (I-V) curves.

It has been reported that ohmic behavior dominates the conduction in these films at low electric (E) fields while Poole-Frenkel emission dominates at higher values of E-field [Maeda et al., 1989]. The E-field value at the transition between these two mechanisms is dependent on the process conditions and is in the order of 10^5 Vcm^{-1}. The room temperature resistivity was found to increase as the [Si]/[N] ratio decreases [Dun et al., 1981; Sinha and Smith, 1978].

C-V characteristics of Metal/Nitride/Semiconductor (MNS) structures usually show negative flat-band voltages (V_{FB}), indicating the existence of a net effective positive charge at the interface and/or in the bulk of the film [Gupta et al., 1991]. The C-V curves also exhibit hysteresis. The magnitude of hysteresis was found to be smaller for N-rich films [Lau et al., 1989]. The maximum capacitance values from the C-V curves, after correction for series resistance, are usually used for computation of static dielectric

constant, ε. For films deposited onto Si substrates, the ε values varied from 5 to 8 with T_S in the range 25-500 ^{0}C at a fixed silane concentration [Kuwano 1969].

Typical bulk electron trapping rates for silicon nitride are so large that they have been intentionally used in memory devices. However, Jones [1985] reported that intentionally deposited nitrogen-rich PECVD nitride films have less charge trapping problems than films that are Si-rich. According to Lau et. al. [1989], Si-rich nitride films display a large and symmetric hysteresis loop in the capacitance-voltage (C-V) curve and a large flat-band voltage shift (ΔV_{FB}) under bias-temperature stress. They

postulated that in these Si-rich nitride films, the dominant defects are Si dangling bonds that can trap both electrons and holes. On the other hand, N-rich nitride films have much smaller and asymmetric hysteresis loop in C-V curve and smaller ΔV_{FB} under bias-temperature stress, indicating that Si dangling bonds, which can trap either electrons or holes, are greatly reduced in N-rich films and the dominant residual traps are hole traps.

Recently, Park et. al. [1993] demonstrated that the bulk trapping rates in Si-H free N-rich nitride films deposited under amino-saturated plasma conditions are significantly lower than those of stoichiometric LPCVD and PECVD nitrides. They found that these rates were, in fact, less than those observed in plasma-deposited silicon oxides produced with high He dilution.

Many variations to the PECVD process have been proposed to reduce the interface trap density of the PECVD silicon nitride/silicon interface, as it is typically at least an order of magnitude higher than that of the thermal oxide/silicon interface [Gereth and Scherber, 1972]. So far no method has been unilaterally successful, although Lu et. al. [1995] have succeeded in obtaining interface trap densities as low as around 10^{10} $cm^{-2}eV^{-1}$. They employ a combination of remote PECVD (RPECVD) and post-deposition rapid thermal annealing (RTA) process (at 900 ^{0}C) to obtain device quality interfaces. Also, the Si-substrates stripped of native oxide are exposed to oxygen plasma prior to nitride film deposition to enable the formation of a 0.5-0.6 nm thickness oxide layer. The details of this procedure are described in Lu et al. [1995]. Another approach adopted by Ma et. al. [1993] to overcome the problem of poor interface is the use Oxide-Nitride-Oxide (ONO) dielectrics where they again combine RPECVD and RTA processes to obtain device quality dielectrics. Ammonia plasma treatment of Si

surface prior to nitride deposition has been found to reduce interface state density of nitride/silicon interface to about 10^{10} $cm^{-2}eV^{-1}$ [Arai et al., 1988]. This improvement is attributed to nitrogen incorporation into the near surface region of the Si-substrate. The suitability of any of these techniques has to be evaluated for the specific application at hand.

1.4.2 Silicon Oxynitride Films

Converting plasma nitride to oxynitride film by introducing oxygen improves thermal stability, cracking resistance, and decreases film stress [Nguyen 1984] all of which may directly affect the usefulness of a dielectric deposition process employed in TFT production due to the large substrate areas involved. It is also reported that oxynitride films (refractive index, n = 1.75-1.8) with oxygen concentration of 16-20 % atomic appear to have better physical and electrical properties compared to other nitride and oxynitride films [Nguyen 1986]. This is attributed in part to a stable amorphous bonding structure in these films. In general, oxynitride layers have properties some where in between those of oxides and nitrides which can be modified easily by varying the film composition through deposition conditions. The variations in the PECVD process detailed in section 1.4.1 are, in general, applicable to oxynitride layers as well.

Overall, it should be kept in mind that the material properties generally cannot be correlated to process conditions independent of reactor configuration.

1.5 Research Objectives

So far in the reported work on PECVD of silicon nitride layers, the SiH_4/NH_3 gas system has been the most popular one with SiH_4/N_2 system drawing some attention.

The latter system results in low hydrogen concentration in the deposited films and typically has lower growth rates compared with the SiH_4/NH_3 system.

The present work is directed towards understanding the process behavior of PECVD of silicon nitride and oxynitride insulator films using disilane (Si_2H_6) as the silicon source, ammonia as the nitrogen source, nitrous oxide as the oxygen source and helium as the diluent gas. This knowledge is utilized in an effort to deposit films with potential application as gate dielectrics in metal-insulator-semiconductor FETs and, in particular, in TFT technology.

1.6 Organization

Chapter 2 deals with the process characterization details of PECVD of silicon nitride layers. The characterization is carried out with respect to process parameters such as the process gas flow ratio, rf input power, process pressure, and substrate temperature. This experiment enables the understanding of the process behavior and also identification of process windows available for deposition of films with the requisite film properties.

Chapter 3 deals with electrical characterization of silicon nitride films deposited under the process conditions derived through the investigation in chapter 2. The electrical properties, obtained from C-V and I-V measurements on MIS structures utilizing silicon nitride films as the insulator, of as-deposited and post-metallization annealed silicon nitride films are presented. These results are compared with the ones known for films deposited using silane. The electrical quality of nitride films deposited on unstripped native oxide is also observed.

Chapter 4 presents the electrical properties of silicon nitride films subjected to different pre- and post-deposition processing conditions. The effects of pre-deposition surface treatment and post-deposition annealing in different gas ambients on the electrical properties of silicon nitride films are detailed.

Chapter 5 deals with the understanding of process behavior of PECVD of silicon oxynitirde films. The deposition is carried out by adding small amounts of nitrous oxide gas to the source gas mix employed for silicon nitride deposition detailed in chapters 3 and 4. The physical, chemical and electrical characteristics of these films are observed with changing nitrous oxide content in the source gas mix, i.e. changing oxygen content in the oxynitride films. These results are compared with the corresponding results for the nitride films.

Chapter 6 gives summary and conclusions.

1.7 Deposition System and Characterization Equipment

The plasma deposition system used for the deposition of various films throughout this work and the equipment to be used for the physical, chemical and electrical characterization of the deposited films will be briefly described in this section.

1.7.1 Plasma Deposition System

Plasma-Therm Wafer/Batch Model 70 plasma deposition system is used for the PECVD of nitride and oxynitride films in this work. This is a microprocessor controlled dual-chamber system, with rf source at 13.56 MHz capacitively coupled to the upper electrode. The bottom electrode is grounded. A detailed diagram of the deposition chamber along with gas supply connections is shown in Fig. 1.6.

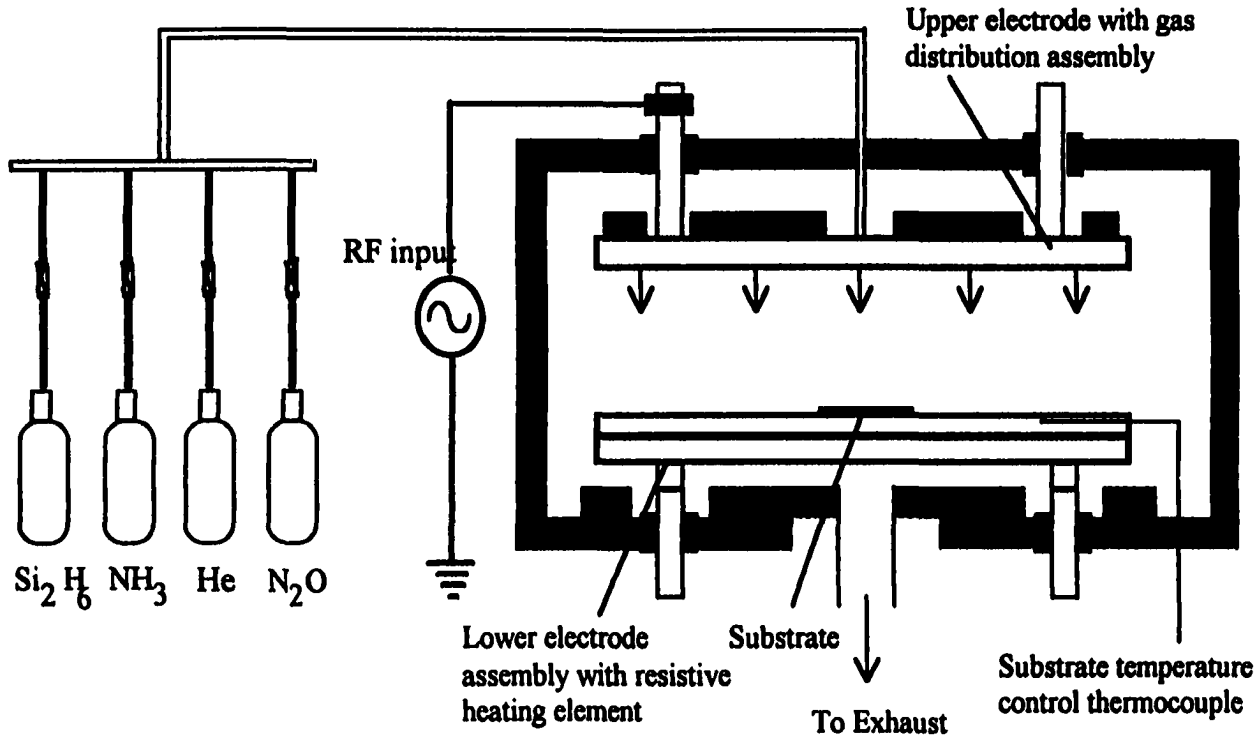


Fig. 1.6. Schematic diagram of the parallel-plate plasma reactor with the gas supply system that is employed in this work. The lower electrode is grounded and the upper electrode connected to 13.56 MHz frequency rf source. The spacing between the electrodes is 1 inch.

1.7.2 Characterization Equipment

Applied Materials Ellipsometer II: An instrument that utilizes the properties of polarized light to measure the thickness and refractive index (RI) of thin films. This ellipsometer uses a He-Ne laser light source at a wavelength of 632.8 nm.

Tencor Instruments Alpha-Step 2000: This profiling equipment uses mechanical stylus method and is used for film thickness measurement upon selective etching of the deposited films in BHF to produce a step-like profile.

Nanometrics 210XP: An instrument that works based esentially on the same principle as the ellipsometer, this will be used to cross-check the thickness data obtained from the above two methods.

Perkin-Elmer Model 1600 Fourier Transform Infrared (FTIR) spectrophotometer: This will be used to obtain FTIR plots for investigation of bonding arrangement in the films. This instrument has a resolution of 4 cm^{-1}.

Hewlett-Packard HP 4275A multi-frequency LCR meter, HP 4140 picoammeter/dc source, and Keithley 490 quasi-static C-V meter: These will be used to obtain high-frequency and quasi-static C-V curves for the Metal/Insulator/Semiconductor structures, with the deposited nitride and oxynitride films employed as the insulator layer. HP 4140 is used to generate the I-V curves of the MIS structures. The constant voltage stressing experiments to obtain charge trapping information will be performed with the HP 4140/HP 4275A.

CHAPTER 2. SILICON NITRIDE FILM DEPOSITION[1]

2.1 Introduction

Plasma depositions are actually low pressure gas polymerization reactions where electron energy in the plasma is utilized to dissociate the precursor molecules to create highly reactive radicals that through gas phase and/or surface reactions produce the desired films. Currently, PECVD silicon nitride films are usually obtained by using silane (SiH_4) as the silicon source and either NH_3 or N_2 as the nitrogen source. Disilane (Si_2H_6) has been known to give better processing thermal budget for low temperature silicon [Yoshikawa and Yamaga, 1986] and SiO_2 [Mishima et al., 1984] film deposition. Recently Song et al. [1995] have reported PECVD of SiO_2 films using Si_2H_6 as silicon source demonstrating better chemical and electrical properties of these films deposited at 120 ^{0}C than those of films deposited using silane or tetraethylorthosilicate (TEOS) at higher temperatures. Disilane requires lower activation energy than silane [Roenigh et al., 1987] and the two silyl radicals generated from plasma dissociation of disilane molecule have a large amount of excess energy making them highly reactive [Oikawa et al., 1994]. This situation is different from the decomposition of silane, where a large amount of the excess energy is shared by the H atom, but only a little by the silyl radical [Tsuda et al., 1985]. These two gas phase dissociation reactions are represented below:

$$SiH_4 \text{ in plasma} \longrightarrow {}^{\bullet}SiH_3 + {}^{\bullet}H$$

[1] Figures in this chapter are reprinted with permission from Journal of Vacuum Science and Technology B. Copyright 1998, American Vacuum Society.

$$Si_2H_6 \text{ in plasma} \xrightarrow{\approx 1e} (Si_2H_6)^*$$

$$(Si_2H_6)^* \longrightarrow 2\ ^{\bullet}SiH_3$$

The presence of highly energetic silyl radicals could potentially increase the precursor formation rate with available radicals or atoms from other source molecules, and thereby increase film deposition rate in mass flow limited regime of PECVD process.

The process variables such as gas flow ratio of NH_3 to disilane (Si_2H_6), process pressure, rf input power, and deposition temperature effect the film deposition in a PECVD process. Understanding the effect of these process variables is crucial not only to gain an insight into the process chemistry but also to be able to deposit films with the requisite film properties in a controlled and repeatable fashion. The effect of these process variables on various film properties of interest would have to be studied to identify process parameter windows that result in deposited films with the desired properties.

In this chapter, the process details for the deposition of PECVD $Si_xN_y:H_z$ films in $Si_2H_6/NH_3/He$ gas system are reported for the first time. Helium is used as the dilution gas with a flow that is 2-3 orders of magnitude higher than that of the disilane. Although this results in reduced deposition rate, the benefits of dilution with helium, an inert and light gas, in terms of suppression of gas phase nucleation, better thickness uniformity of films deposited and reduced plasma-induced damage at the film-substrate interface are generally well known [Batey and Tierney, 1986]. The process characterization was carried out with the gas flow ratio, pressure, substrate temperature and rf power as the variables. Deposition rate, etch rate, refractive index and bonding configuration in the films were examined as a function of different process parameters.

2.2 Experiment

The apparatus used for film deposition is a conventional parallel plate plasma reactor described in chapter 1 (section 1.7.1). The substrate is placed on the grounded bottom electrode. The substrate temperature can be controlled up to 300 ^{0}C by resistive heating. The upper electrode was always maintained at 60 ^{0}C. Boron doped, chemically-polished 4" diameter 5-10 Ω-cm Si wafers of (100) orientation were used as the substrates. After loading the wafers, the chamber was pumped down to a base pressure of 3 x 10^{-4} Torr. The process gases used were 5% Si_2H_6 in a He base, 99.9995% purity NH_3 and 99.999% purity He. The deposition recipe in detail is shown in Fig. 2.1. A flow rate of 500 sccm was maintained for He unless otherwise mentioned. N-rich silicon nitride films have been reported in earlier works to have superior electrical characteristics compared to both stoichiometric and Si-rich films [Jones 1985; Lau et al., 1989]. For this reason, in this experiment, unless otherwise mentioned, an ammonia to disilane flow ratio of 20 was chosen to deposit N-rich films. As the dissociation energy of ammonia is higher than that for disilane, an rf power of 50 W was required at this flow ratio to achieve sufficient dissociation of ammonia to be able to deposit N-rich films. These process details would be later related to electrical properties of these silicon nitride films. The thickness of the deposited films was measured by an ellipsometer with 632.8 nm He-Ne laser and a Nanometrics 210 XP thickness meter. The etch rates were measured in 1:10 volume ratio of BHF:H_2O solution. The FTIR spectra were recorded with a Perkin-Elmer 1600 spectrophotometer with 4 cm^{-1} resolution using a bare Si sample for background subtraction. The thickness of the films

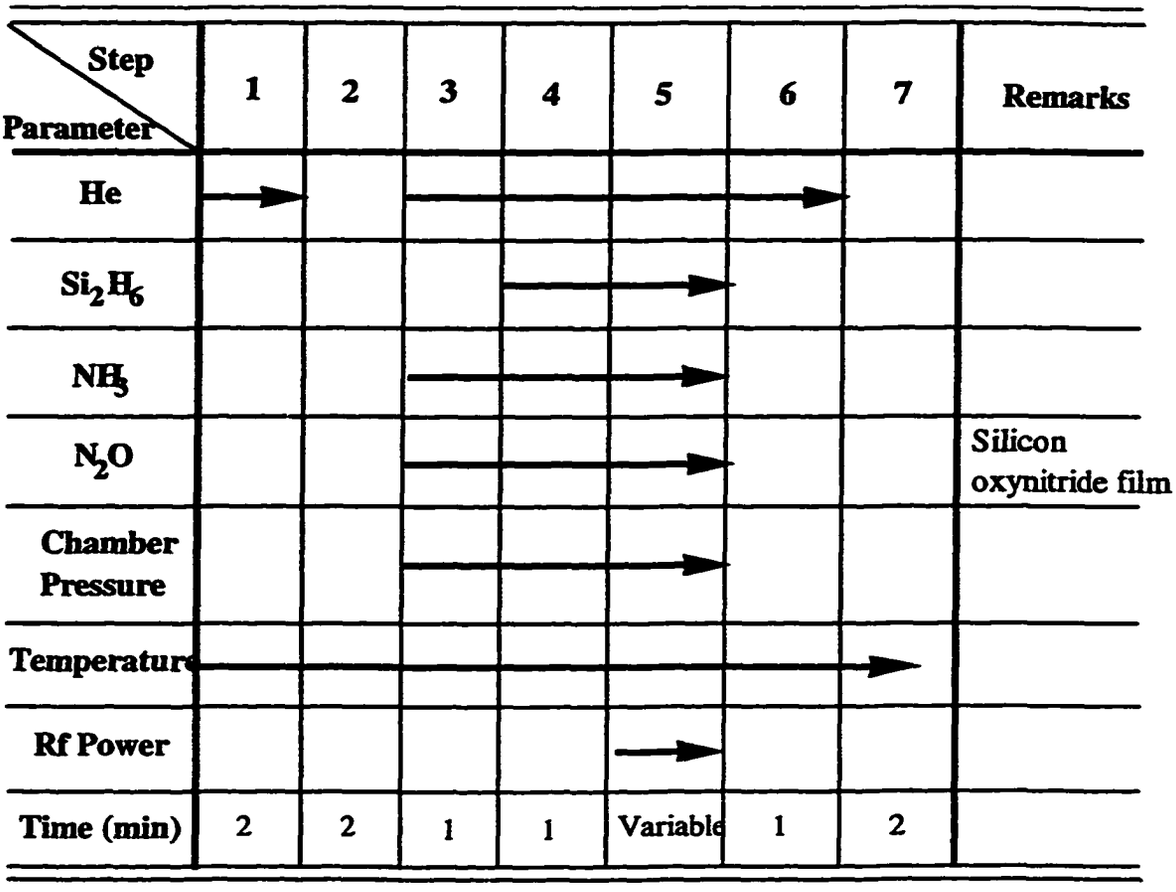


Fig. 2.1. The detailed recipe for the deposition of silicon nitride and oxynitride films in the $Si_2H_6/NH_3/He$ and $Si_2H_6/NH_3/N_2O/He$ gas systems respectively. The process chamber is pumped down to base pressure before commencing step 1. The film deposition is carried out during step 5.

used for FTIR measurements was within the range 215 ± 5 nm. The relative H concentration in arbitrary units, $[H_{rel}]$, in the films is deduced from the FTIR spectra by integration of the N-H and Si-H bond absorbance peaks centered around 3350 and 2160 cm^{-1}, respectively, and using the equation:

$$[H_{rel}] = [Si\text{-}H] + 1.4\,[N\text{-}H] = \int_{2160} A(\omega)\,d\omega + 1.4 \int_{3350} A(\omega)\,d\omega$$

where $A(\omega)$ is the absorption in arbitrary units at frequency ω. The factor of 1.4 was suggested by Lanford and Rand [1978] due to the higher absorptivity of the Si-H band compared to that of the N-H band.

2.3 Results and Discussion

Silicon nitride deposition rate is plotted in Fig. 2.2 for two different rf powers, 50 and 100 W, with varying flow ratio of disilane to ammonia. The process pressure was 700 mTorr and the substrate temperature was 250 ^{0}C. Two regions of operation namely the excess-ammonia regime and the excess-disilane regime are apparent in this figure, as in the case of silane chemistry [Smith 1993]. In the excess-ammonia regime at low values of disilane to ammonia flow ratio, most of the silicon from the precursor disilane molecule is utilized towards film deposition due to the availability of an excess number of nitriding radicals created from ammonia. The films deposited in this regime are N-rich, as will be also confirmed later from IR spectra. In the excess-disilane regime at higher values of disilane to ammonia flow ratio, there are not enough $NH_{n<3}$ radicals to fully nitride the silyl radicals created from the disilane molecules, and this results in saturation of the growth rate. The critical ratio of rf power to disilane flow rate F_C that demarcates the two regimes is ~40 W/sccm for the deposition system used in this work.

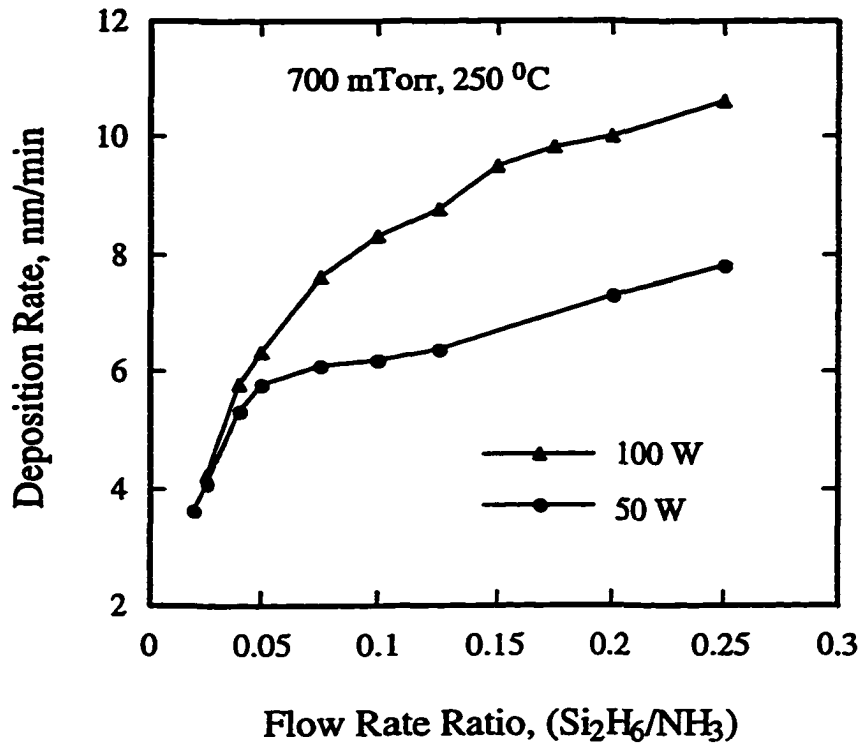


Fig. 2.2. Deposition rate of silicon nitride films as a function of disilane to ammonia flow ratio at two different rf powers. The total flow was maintained at 520 sccm with helium flow rate at 500 sccm. The F_C value for this system is ~ 40 W/sccm.

The finite non-zero slope of the deposition rate curve in this region (Fig. 2.2) is due to the simultaneous deposition of a-Si:H from the excess disilane molecules.

Figure 2.3 shows the FTIR spectra of seven different silicon nitride samples deposited under varying flow ratio conditions. The rf power for this deposition was 50 W. The spectrum for the film deposited with a flow ratio R of ammonia to disilane of 20 shows absorbance bands related to N-H stretching (3350 cm^{-1}), N-H bending (1170 cm^{-1}) and Si-N stretching (870 cm^{-1}) vibrations. There is no observable Si-H stretching (2160 cm^{-1}) absorption. With no observable Si-Si bonding, at 600 cm^{-1}, it can be concluded that this film is N-rich. As the flow ratio R decreases i.e. with increasing disilane flow, the N-H bond area decreases and the Si-H band, after first appearing in films deposited with flow ratio of 10, continues to grow in size.

The H-concentration in these films is plotted in Fig. 2.4 as a function of ammonia/disilane flow ratio. The total H concentration in these films is found to be nearly constant in the range of flow ratios investigated. Lu et al. [1995] reported U-shaped curves for total H concentration for silane based films where the H concentration was high for very low and very high flow ratios with a broad minimum for intermediate flow ratios. Although, in our work, care was taken to cover a wide range of flow ratios, this U-shaped behavior was not observed. The central broad minimum was the only region observed here over a flow ratio range higher than that investigated by Lu et al. [1995].

Figure 2.5 shows the deposition and etch rates of the nitride films as a function of process pressure. The ammonia to disilane flow ratio and rf power were 20 and 50 W respectively. As seen from this figure, the deposition rate is insensitive to variations in process pressure. A similar trend is also reflected in the etch rates of the films up to a

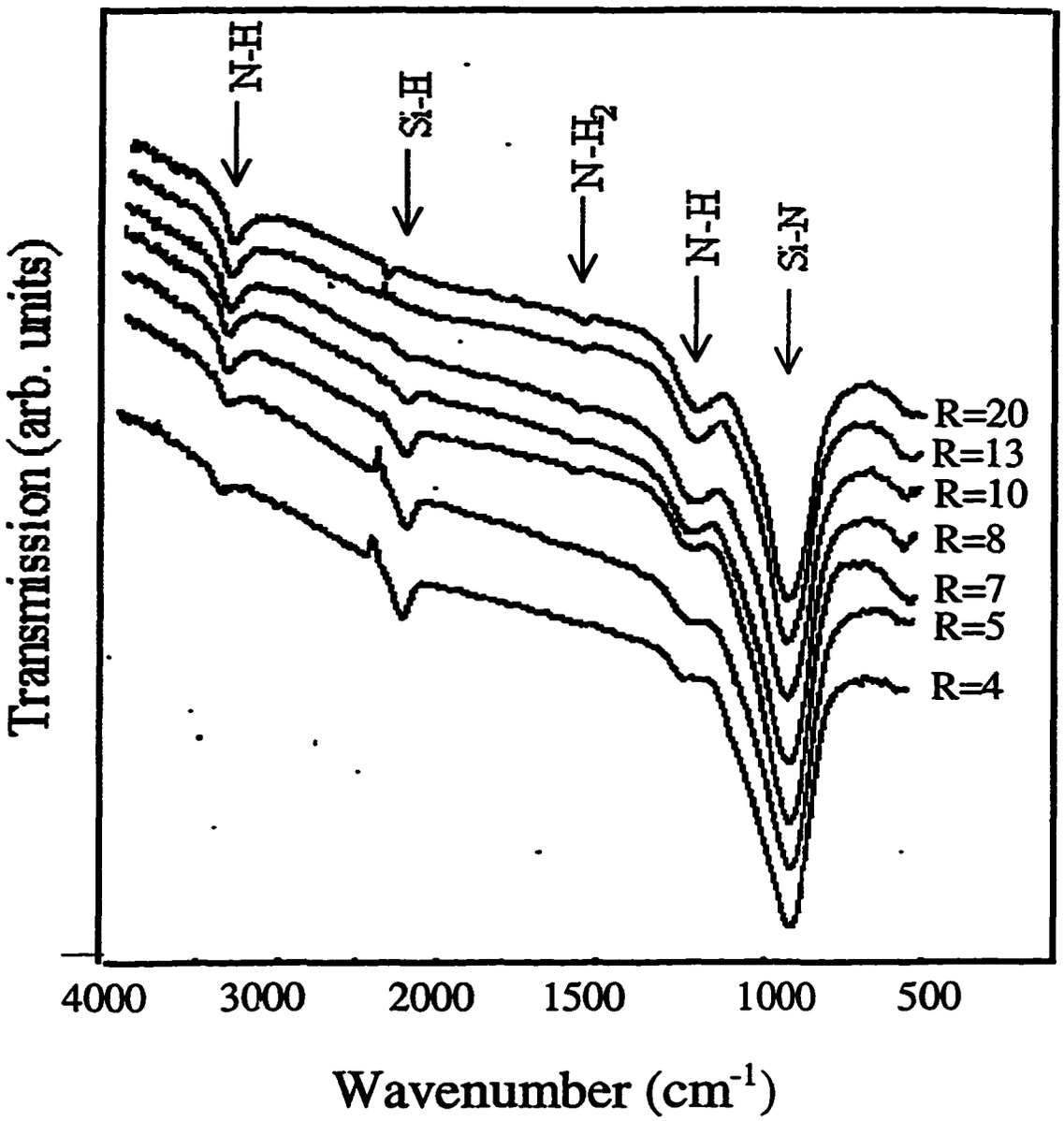


Fig. 2.3. Infrared transmission spectra of the silicon nitride films as a function of flow ratio, R, of ammonia to disilane. Rf power = 50 W, process pressure = 750 mTorr, and substrate temperature = 250 ^{0}C. The arrows indicate the location of the absorption peaks in the vibrational spectrum. The vertical scale for each curve is offset for clarity.

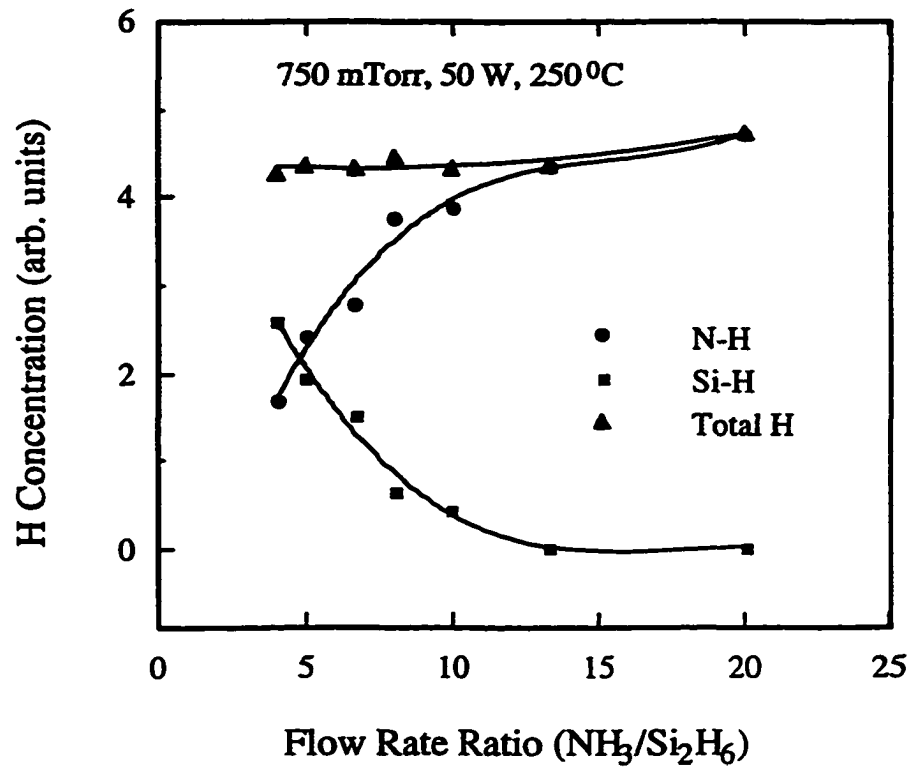


Fig. 2.4. Total bonded H concentration in the silicon nitride films as a function of flow ratio of ammonia to disilane.

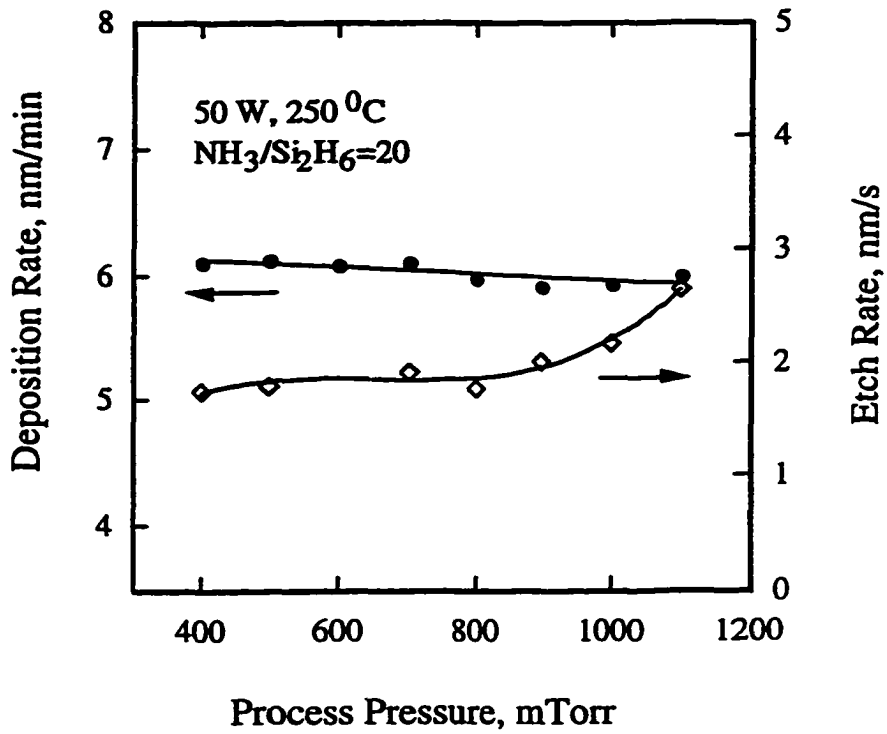


Fig. 2.5. Deposition and etch rates of the silicon nitride films as a function of the process pressure.

deposition pressure of 1 Torr with etch rate increasing at pressures higher than 1 Torr. From this it can be concluded that the film composition and density are not dependent on the process pressure over a wide range. This is partly due to the dilution of the process gases with large amounts of helium.

Figure 2.6 examines the deposition rates as a function of rf power for three different process pressures: 300 mTorr, 750 mTorr and 1100 mTorr. The flow ratio of ammonia to disilane was 20. Two most salient features of the observed behavior are: i) for the flow ratio of 20, about 50 W of rf power completely utilizes the silicon in the disilane precursor molecule as observed in Fig. 2.2; and ii) the constancy of deposition rate with process pressure is valid only below this critical-power. At power levels higher than this, higher pressure results in higher deposition rates. This is very likely due to the longer gas residence time in the reactor at higher pressure, which allows more time for the source gases to become activated and also for the reactants to diffuse to the substrate before being swept out.

The influence of substrate temperature on the deposition and etch rates is plotted in Fig. 2.7. The different depositions were carried out at 750 mTorr pressure with gas flow ratio of 20 and rf power of 50 W. The deposition rate decreases from 7.2 nm/min at 60 ^{0}C to 5.9 nm/min at 270 ^{0}C, about an 18% decrease over the temperature range covered. This decrease is smaller than the reported value of over 50% for the same temperature range for silane based films [Lee et al., 1993]. Film densification at higher substrate temperatures is believed to be responsible for a decrease in the deposition rates with increasing temperature. Low deposition rates utilized in this work may imply longer time for the surface adsorbent molecules for surface phase reactions and/or for selecting suitable surface bonding sites. Hence the substrate temperature may not play as

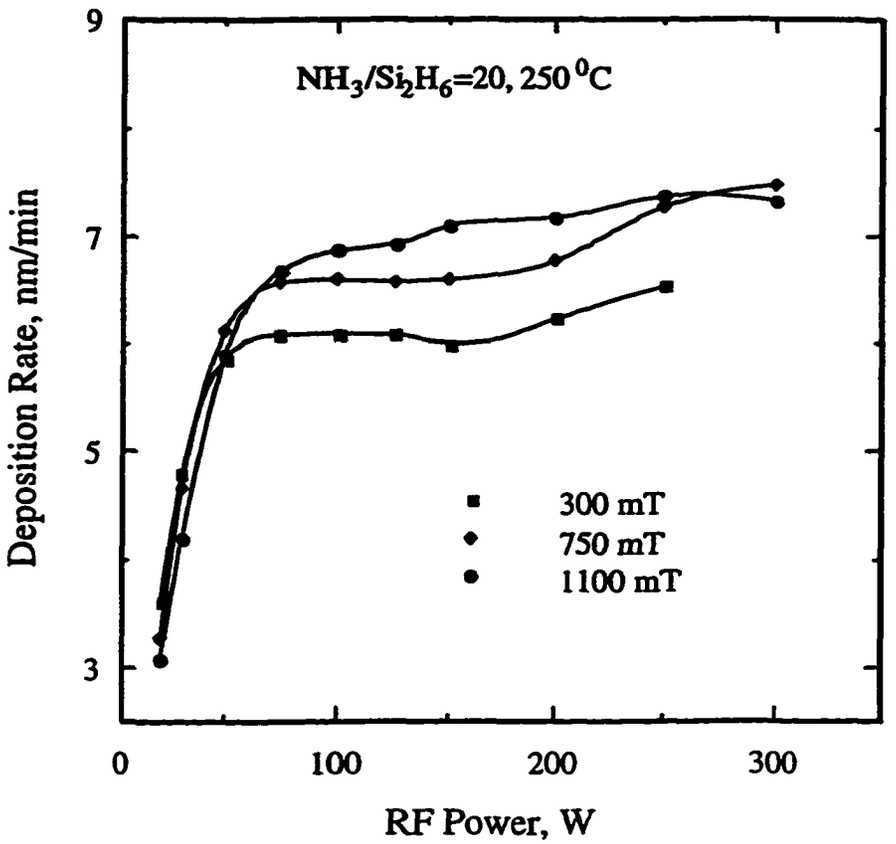


Fig. 2.6. Deposition rate of the silicon nitride films as a function of rf input power for three different process pressures. The total flow rate was held constant.

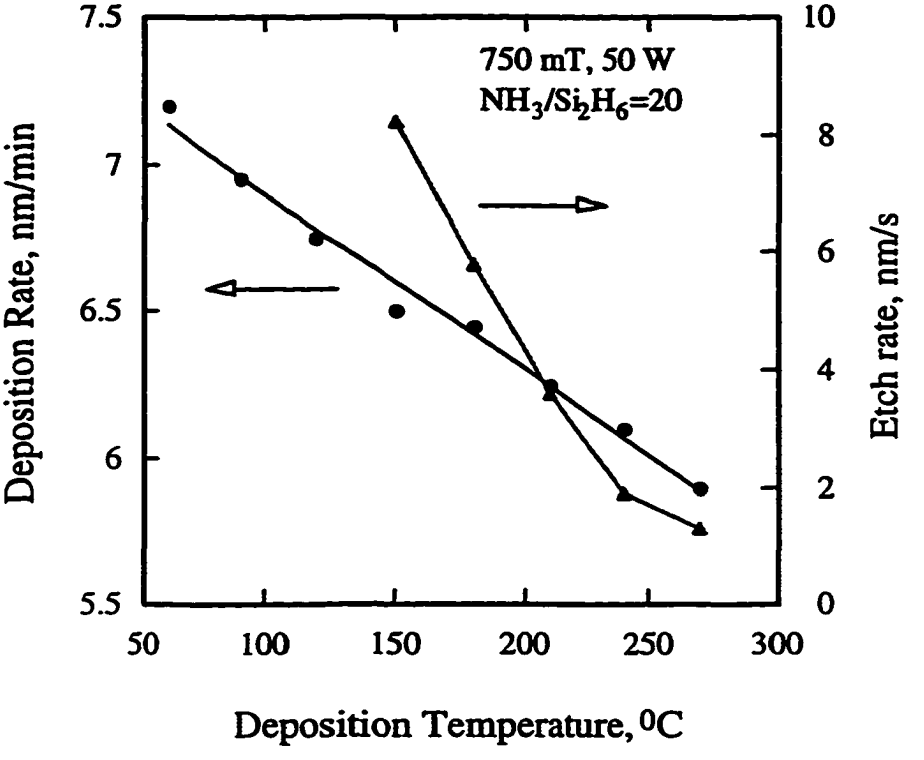
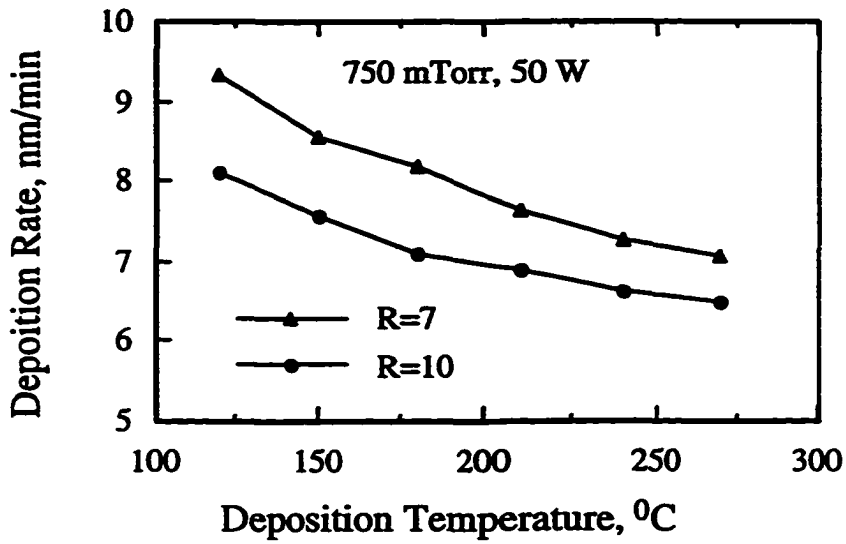


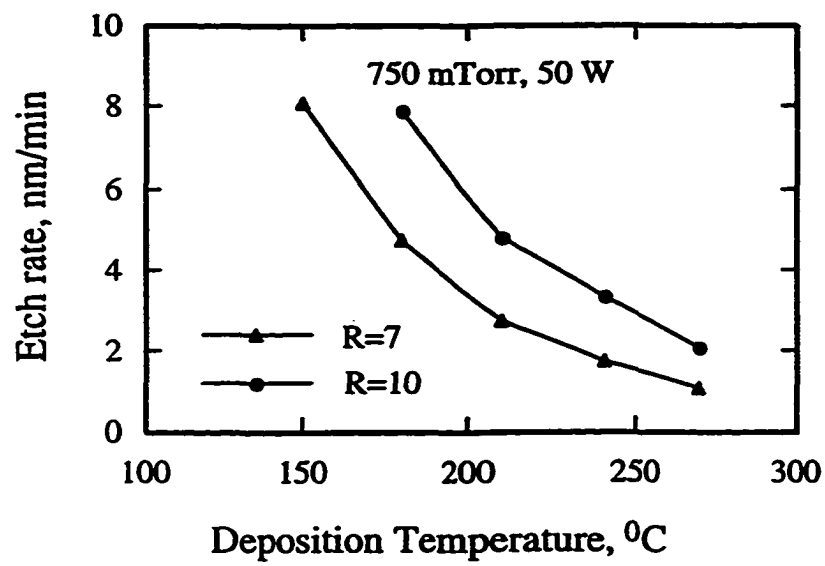
Fig. 2.7. Deposition rate of the silicon nitride films as a function of substrate temperature.

important a role in film densification. However, as is seen later, the film composition and especially the H concentration of the films are still a function of the deposition temperature. This is also evident from the etch rate of the films deposited at different temperatures. The etch rate increases sharply for films deposited at temperatures below 240 ^{0}C indicating lower density and higher H concentration of these films. Films were deposited at varying temperatures at two different ammonia to disilane flow ratio values of 7 and 10. All other process conditions were kept the same as the ones for Fig. 2.7. The deposition and etch rates of these films as a function of temperature are plotted in Fig. 2.8. Deposited in the disilane-rich regime, these films were Si-rich with values for refractive index between 1.9 and 2. The etch rates of these films decreases with increasing deposition temperature, a trend that is seen with all plasma deposited silicon nitride films [Gupta et al., 1991. Films deposited at lower flow ratios have lower etch rates owing to the higher Si content in the films.

The stress and the thermal stability of PECVD silicon nitride films are strongly dependent on the H concentration in the films. Hydrogen evolution is known to occur in Si_xN_y:H films upon thermal annealing with H evolving first from Si-H bonds due to its lesser resistance to thermal heating and then from N-H bonds [Nguyen 1986]. The resultant charge traps in the silicon nitride films are dependent on the number of dangling bonds in the films which in turn depends upon the initial H concentration, H bonding configuration and the film annealing conditions. FTIR spectroscopy was employed to analyze the H concentration of films deposited at different temperatures. Fig. 2.9 shows the IR transmission spectra of these films. Having been deposited in the ammonia-rich regime, these films do not exhibit Si-H absorbance band at 2160 cm^{-1}. The integrated N-H band area was used to plot the relative H-concentration in these



(a)



(b)

Fig. 2.8. Deposition (a) and etch rates (b) of the silicon nitride films as a function of deposition temperature for two different flow rate ratio R of ammonia to disilane values of 7 and 10.

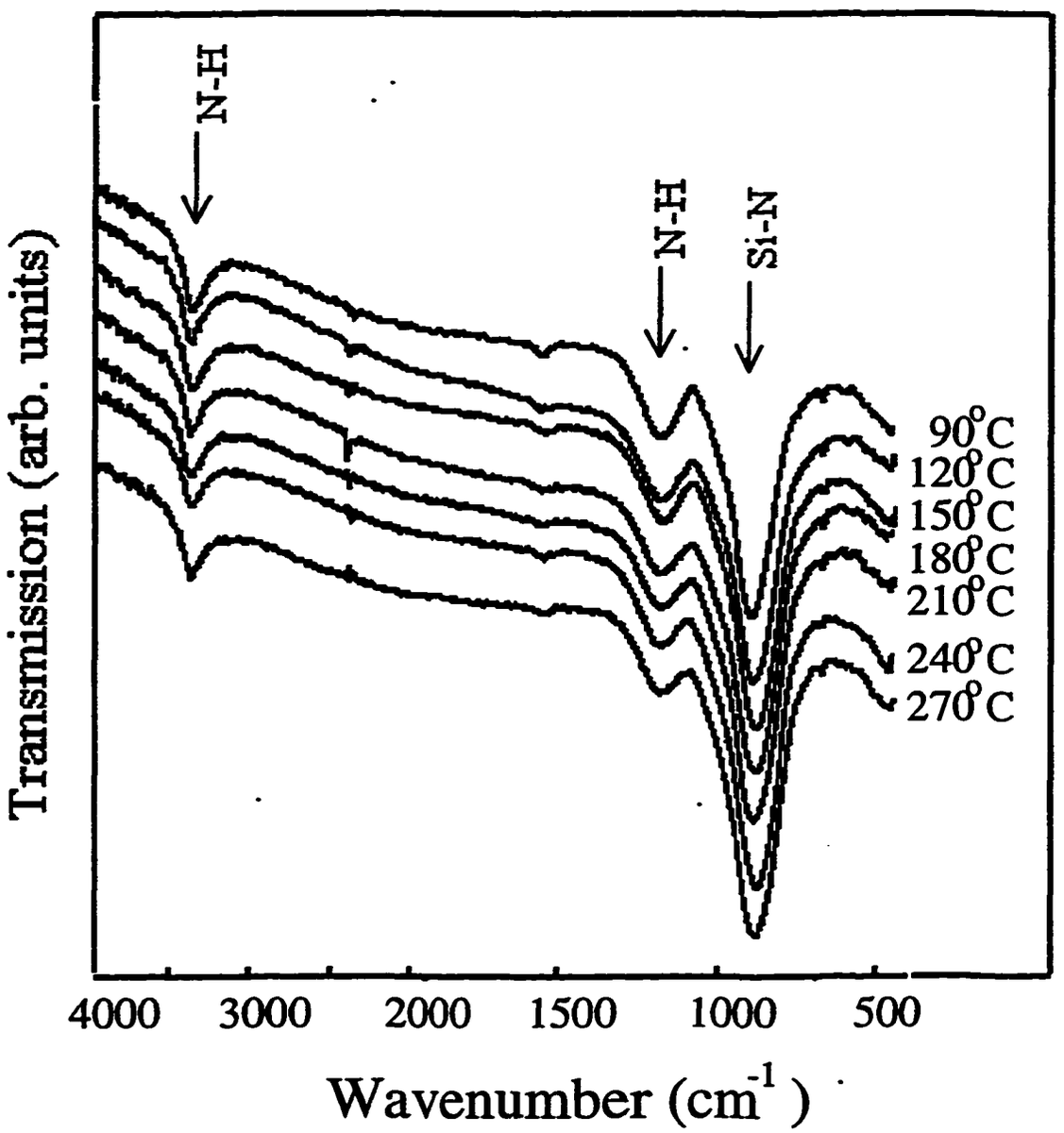


Fig. 2.9. Infrared transmission spectra of the silicon nitride films deposited at substrate temperatures in the range of 90 ^{0}C - 270 ^{0}C. Flow ratio R = 20, rf power = 50 W and process pressure = 750 mTorr. The vertical scale for each curve is offset for clarity.

films as a function of substrate temperature as shown in Fig. 2.10. The change in H concentration with substrate temperature was found to be more gradual than is usually observed in silane based films [Gupta et al., 1991]. This in fact is evident from Fig. 2.9 where the N-H stretching band (3350 cm^{-1}) area seems fairly constant for the plotted range of temperatures.

2.4 Summary and Conclusions

The characterization details for plasma enhanced chemical vapor deposition of silicon nitride films with disilane as silicon source are reported for the first time. Despite large dilution of process gases with helium and small amounts of disilane used (typically about 1 sccm), respectable deposition rates were achieved. Similar to silane-based film growth case, two regimes of deposition, namely the excess-ammonia regime and excess-disilane regime, were also observed for the disilane case. Films deposited under process conditions *falling at the boundary of these two regimes* had deposition rates that were mostly dependent on rf power and gas flow ratio resulting in uniform and highly repeatable film qualities. Films deposited under these conditions were N-rich which have been reported in earlier works to have superior electrical characteristics compared to both stoichiometric and Si-rich silicon nitride films. The H concentration in these deposited films was found to be nearly independent of the gas flow ratio over the range investigated. Also, the variation in deposition rate and H concentration of the films with deposition temperature was considerably smaller than has been reported for silane based films. These process details were used to choose the eventual set of process parameters to be used for the deposition of silicon nitride films. A relatively low rf power of 50 W was chosen to have good thickness uniformity and also to avoid plasma-induced damage that occurs at high rf powers. The gas flow ratio was chosen to attain

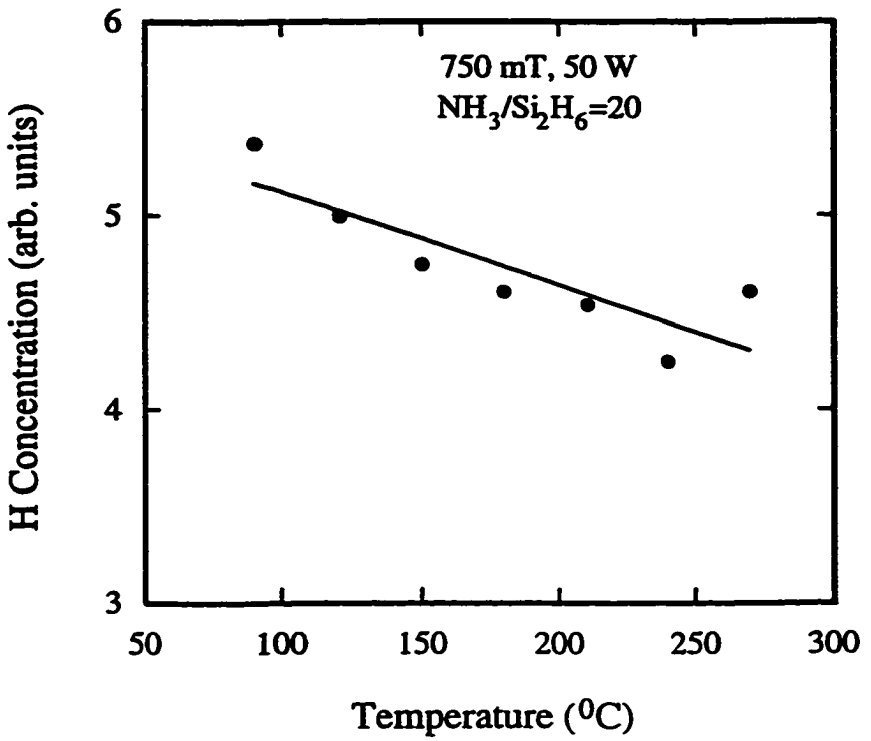


Fig. 2.10. Total bonded H concentration in the silicon nitride films as a function of substrate temperature. This data is derived from the IR spectra of the same films plotted in Fig. 2.9.

maximum utilization of disilane at this rf power and also to have the highest deposition rate possible with the resultant films being N-rich. All these conditions were realized for the films deposited at the boundary of the excess-ammonia and excess-disilane regimes discussed above. The ammonia to disilane flow rate ratio to meet these conditions was 20 in our work. The process pressure under these conditions was not found to have significant effect on the film deposition rate and the film quality. A process pressure of 750 mTorr was chosen for the depositions in the reactor used in this work. The choice of deposition temperature was based on obtaining low H concentration in the films and was chosen as 250 ^{O}C. The thickness uniformity variation of the silicon nitride films deposited under these conditions as measured by ellipsometer was < ±3% across 4" diameter wafers.

CHAPTER 3. ELECTRICAL PROPERTIES OF SILICON NITRIDE FILMS

3.1 Introduction

As discussed in chapter 1, the suitability of PECVD silicon nitride films as a gate dielectric in metal-insulator-semiconductor FETs (MISFETs) and thin film transistors (TFTs) has received much attention only recently upon recognition that nitrogen-rich PECVD films have superior electrical properties such as higher breakdown voltage [Kanicki 1988], smaller bulk charge density and less severe charge trapping problems [Lu et al., 1989]. Since then many subtle variations of the plasma deposition process and/or additional processing steps with moderately high thermal budget have been proposed to realize device quality silicon nitride films [Yasui et al., 1994; Arai et al., 1988; Lu et al., 1995]. In this chapter, the electrical properties of the silicon nitride films deposited under process conditions identified in chapter 2 are presented. A comparison is made between the available information on the typical electrical properties of nitride films deposited in silane-based gas systems and the results from this work on nitride films deposited in a disilane-based system.

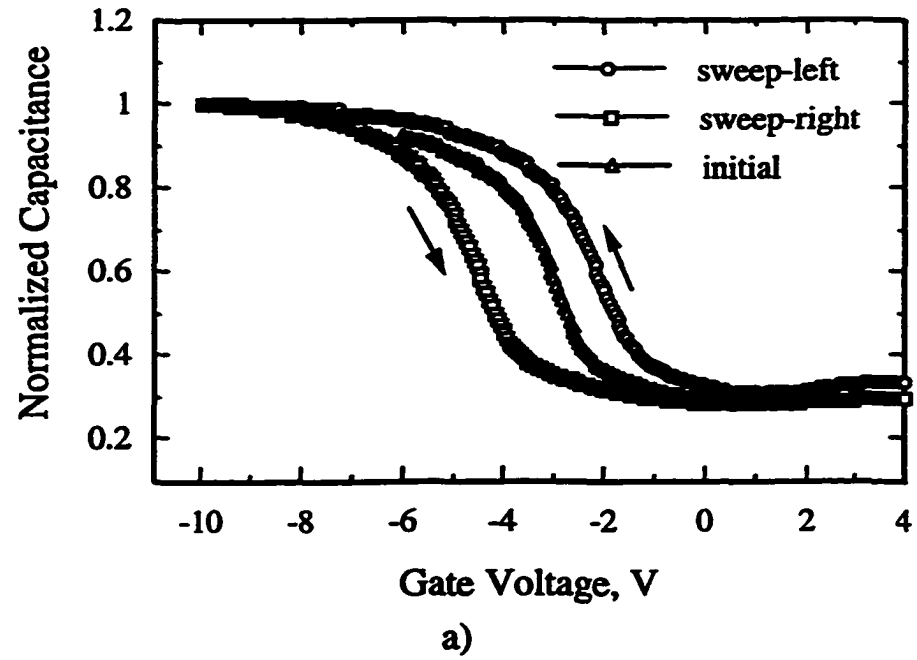
3.2 Experiment

Chemically polished 4 in. diameter boron doped Si wafers with 100 orientation and 5-10 Ω-cm resistivity are used as the substrates. The process gases are 1 sccm of Si_2H_6, 20 sccm of NH_3, and 500 sccm of He. The process pressure and rf power are 750 mTorr and 50 W, respectively. The substrate temperature is maintained at 250 ^{0}C. Silicon nitride films with 100 nm thickness are deposited at a rate of 5.5 nm/min with

thickness variation of $\leq \pm$ 3% across 4 in. diameter wafers. The conventional RCA cleaning followed by 1 minute dip in 100 : 1 volume ratio of DI water : HF(48%) solution, unless otherwise mentioned, is used as the predeposition cleaning procedure. Some wafers are not stripped of the native oxide prior to the deposition to examine its effects on the film properties. The plasma chamber was pumped down to $1x10^{-5}$ Torr base pressure after loading the samples and before commencing the deposition process using a turbo pump backed by a roots blower and a mechanical pump. This is lower than $3x10^{-4}$ Torr pressure used in chapter 2 to provide purer films. The thickness of the films is determined by ellipsometry. These films are nitrogen rich with no detectable Si-H bonding through infrared spectroscopy analysis. Thermally evaporated Al was used as the gate material for the metal-nitride-semiconductor (MNS) capacitors. Standard photolithography technique was employed in preparing these capacitors with gate area of $2.3x10^{-3}$ cm^2. To ensure proper contact to the substrate, Al is evaporated on the back side of the substrates. Post metallization anneal (PMA) is carried out at 400 ^{0}C in N_2 ambient for 30 minutes. 1 MHz C-V and ramp I-V curves for these capacitors are obtained using HP 4275 LCR meter and HP 4140 dc source/picoammeter. Keithley 490 quasi-static CV meter is used for acquiring the low frequency C-V curves. High-low frequency capacitance method is used in determining the silicon nitride-Si interface trap density [Castagne and Vapaille, 1971].

3.3 Results and Discussion

Figure 3.1 shows the normalized capacitance of the MNS structures with as-deposited and post-metallization annealed silicon nitride films, as a function of gate bias voltage. A small range gate bias scan was utilized in obtaining the initial C-V curve.



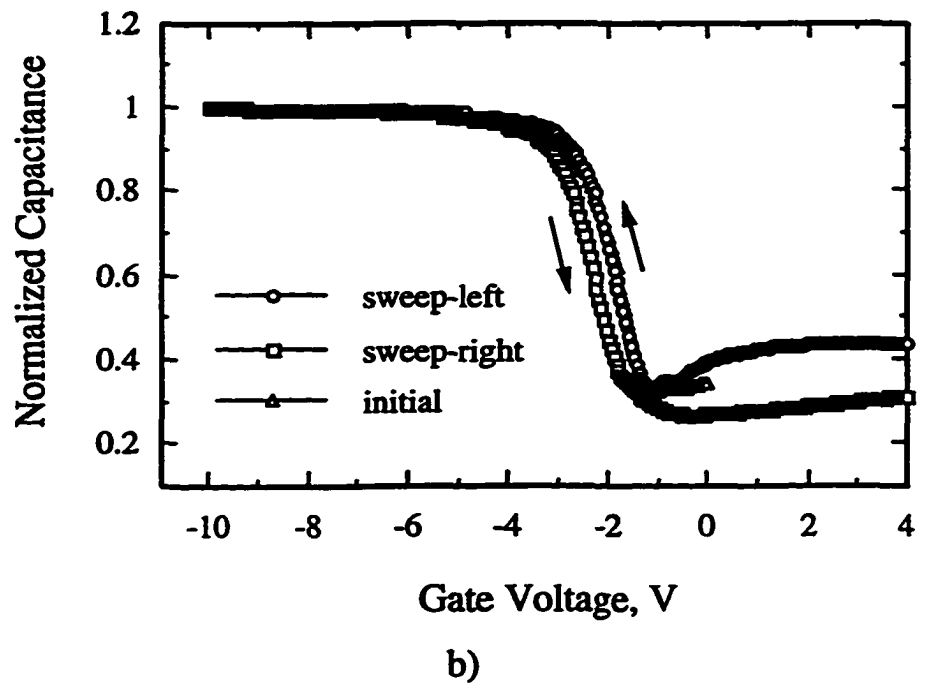


Fig. 3.1. C-V curves for the MNS capacitors at 1 MHz with a) as-deposited and b) post-metallization annealed silicon nitride films. Film thickness = 100 nm and substrate doping density = 1.2×10^{15} cm^{-3}.

Subsequently, a +10 to -10V and a -10 to +10V gate bias sweeps at a sweep rate of 0.02 V/s were used to obtain the 'sweep-left' followed by the 'sweep-right' curve, respectively. The bias was maintained constant for 40 seconds at the beginning of each sweep. The relative dielectric constant ε_r at 1 MHz of both the as-deposited and the annealed films, determined from maximum capacitance in accumulation, was 6.6. The flatband voltages V_{FBi}, V_{FBl}, and V_{FBr} obtained from the initial, sweep-left and sweep-right C-V curves respectively and hysteresis voltage, $V_H = (V_{FBl} - V_{FBr})$ are given in Table 3.1. The net effective nitride bulk and interface trap charge density, Q_F, was evaluated using the formula:

$$Q_F = -C_N(V_{FBi}-\phi_{MS}),$$

where C_N is the capacitance per unit area of the nitride films and $q\phi_{MS}$ is the work function difference between Al gate and semiconductor with q being the magnitude of the electron charge. ϕ_{MS} value for the substrate doping used is 0.88 V. V_H is a measure of the charge instability in the nitride films at room temperature. A positive value of V_H implies instability due to net charge trapping in the nitride films resulting from injection at the semiconductor-insulator interface while a negative value of V_H implies instability due to net ion motion in the nitride film and/or net charge injection at the metal-nitride interface.

From Fig. 3.1 (a), the as-deposited films exhibit V_{FBi} of -3.15 V and also a net negative and a net positive charge trapping under positive and negative gate biases, respectively. This resulted in V_H value of +2.4 V, with the positive sign of V_H indicating net trapping of charges injected from the semiconductor into the nitride film. The curves

Table 3.1. A comparison of various electrical properties of the as-deposited and post-metallization annealed silicon nitride films.

	V_{FBi} (V)	V_{FBl} (V)	V_{FBr} (V)	V_H (V)	Q_F/q (cm^{-2})	D_{it} ($cm^{-2}eV^{-1}$)	E_{DB} (MV/cm)
As-deposited	-3.15	-2.15	-4.55	2.4	8.3×10^{11}	2×10^{12}	7.8
Annealed	-1.8	-1.85	-2.3	0.45	3.3×10^{11}	$2\text{-}3 \times 10^{11}$	7.1

also show a large stretch-out along the gate voltage axis that could be due to both charge injection and poor interfacial properties. The effect of PMA on the C-V curves of the MNS structures is evident upon comparison of Fig. 3.1 (a) and (b). Not only has the magnitude of V_{FBi} reduced to a lower value of -1.8 V, but so has the net charge trapping in the nitride films. In fact, the annealed MNS structures exhibit negligibly small negative charge trapping under applied positive gate bias, resulting in V_H value of 0.45 V. These low values for flatband and hysteresis voltages for 100 nm thick silicon nitride films, resulting from a simple process scheme of 250 ^{0}C deposition and 400 ^{0}C annealing, are lower than the values obtained from silane systems employing similar process conditions [Yasui et al., 1994; Arai et al., 1988]. Also, these values are comparable to the results obtained from silane process schemes that involve higher thermal budgets utilizing rapid thermal annealing [Ma and Lucovsky. 1994] and/or additional process steps like pre-deposition surface treatment in H_2 plasma [Arai et al., 1988] and O_2 plasma [Lu et al., 1995] and hydrogen radical-assisted PECVD [Yasui et al., 1994].

It has been reported earlier [Song et al., 1996] that PECVD silicon oxide films deposited on native oxide free surfaces have five times more effective oxide charge and flatband interface trap densities compared to films deposited on substrates with the native oxide layer. It was also found that 30 minute PMA in N_2 ambient resulted in comparable properties for both kinds of films. In an effort to understand the effect of the presence of native oxide layer on the fixed charge and interface trap density in silicon nitride films, deposition was carried out on Si substrate surface with the native oxidepresent. The 1 MHz C-V curves of MIS structures with these as-deposited and

post-metallization annealed films are shown in Fig. 3.2. The flatband voltages and the fixed charge density of these films are listed in Table 3.2. Both as-deposited and annealed films show high fixed charge densities. Although the hysteresis voltage decreased dramatically for the annealed devices, the flat band voltages were still found to be very high. These high flatband voltages for these devices is a subject matter that will be revisited in chapter 4.

Figure 3.3 shows the interface trap density, D_{it}, of the MNS structures with as-deposited and annealed silicon nitride films of Fig. 3.1. The high-low frequency capacitance technique, valid only till the onset of weak inversion, gives D_{it} information only in the lower half of the bandgap for the p-type substrates used. The D_{it} values reduce by almost an order of magnitude for the annealed interfaces as indicated in Table 3.1. This is also qualitatively evident from the marked reduction in the stretch-out of the corresponding C-V curves in Fig. 3.1. The D_{it} values of 2-3 X 10^{11} $cm^{-2}eV^{-1}$ for the annealed films, though higher by an order of magnitude compared to thermal oxide films, are very respectable for plasma deposited silicon nitride films.

The ramp I-V characteristics of the MNS capacitors give information on the electrical integrity of the dielectric layers and also on the current conduction mechanisms [Sze 1969]. These are shown in Fig. 3.4 for both the as-deposited and the annealed films, where log J is plotted versus $E^{1/2}$. The gate bias was negative with respect to the substrate. This biases the device under accumulation and for $|V_G| \geq |V_{FBi}|$ results in the applied potential mostly dropping across the nitride layer. Both curves shown in Fig. 3.4 are similar, with the annealed films showing lower currents at higher electric fields. The x-axis intercept of the straight-line portion of the $J\text{-}E^{1/2}$ curve for the

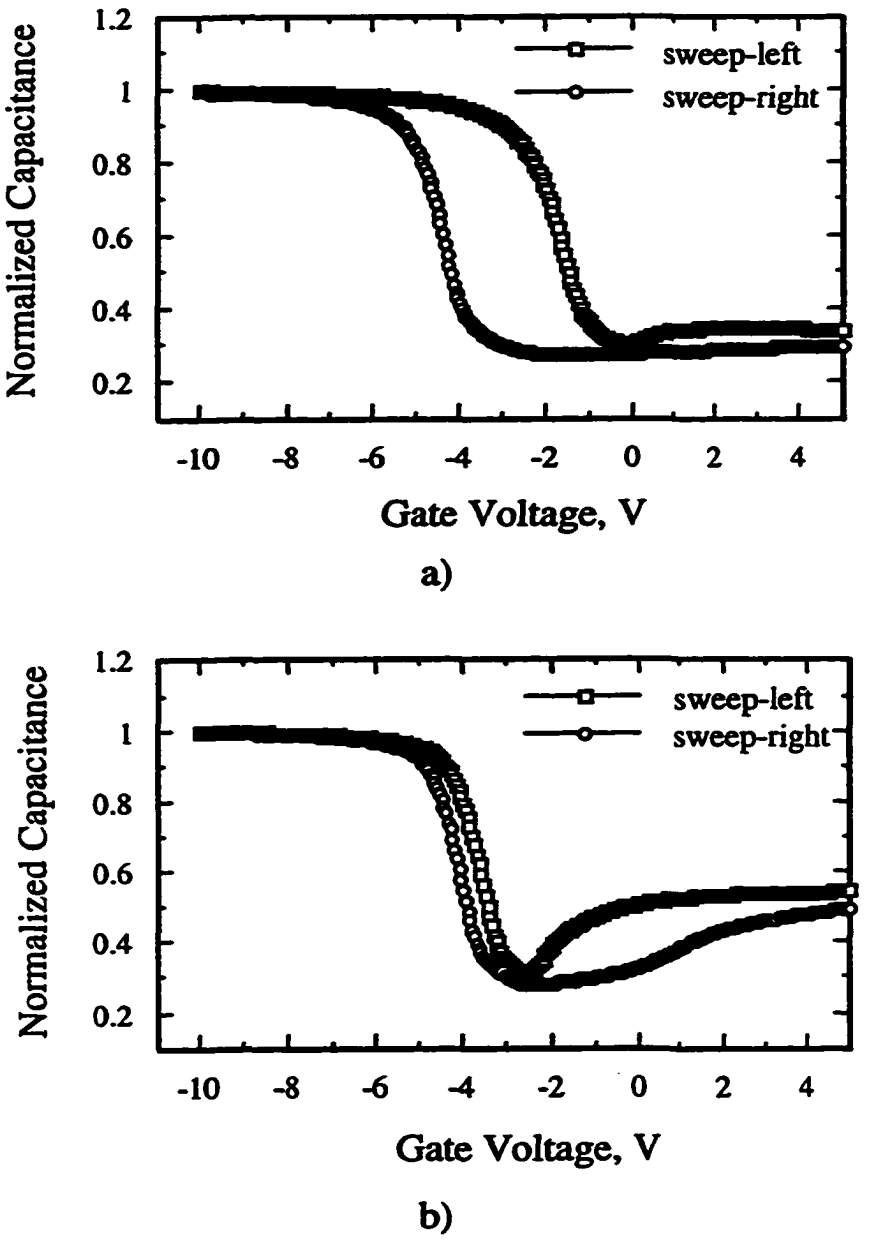


Fig. 3.2. C-V curves for the MNS capacitors with nitride films deposited on native oxide. Fig. a) is for as-deposited and b) is for post-metallization annealed films. Film thickness = 100 nm and substrate doping density = 1.2×10^{15} cm^{-3}.

Table 3.2. A comparison of various electrical properties of the as-deposited and post-metallization annealed silicon nitride films. The Si substrate wafers were not stripped of native oxide prior to the nitride layer deposition.

	V_{FBi} (V)	V_{FBl} (V)	V_{FBr} (V)	V_H (V)	Q_f/q (cm^{-2})
As-deposited	-3.8	-1.6	-4.4	2.8	1.1×10^{12}
Annealed	-3.6	-3.5	-4.05	0.55	1×10^{12}

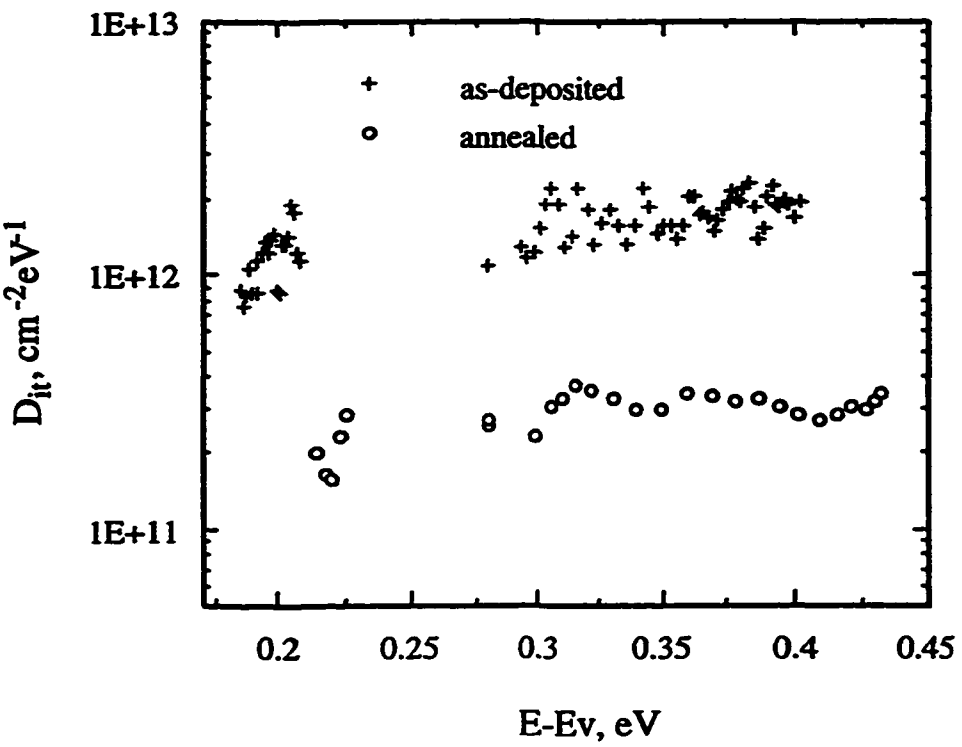


Fig. 3.3. Interface trap density vs position in the silicon bandgap for MNS devices with as-deposited and annealed films.

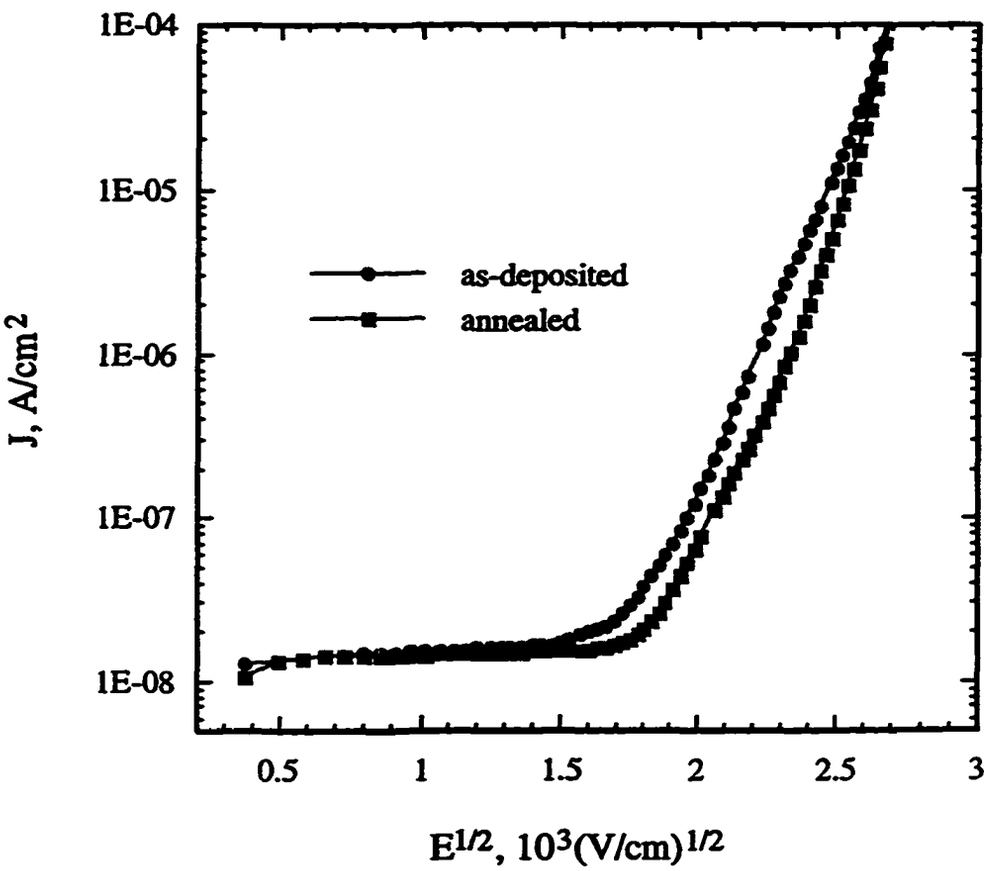


Fig. 3.4. Ramp I-V characteristics of MNS capacitors with as-deposited and annealed silicon nitride films. The ramp rate was 0.25 V/s with gate voltage negative with respect to the substrate. J is current density and E is the average electric field in the nitride layer.

annealed films is larger implying improved interface and lower trap density in the annealed films [Dun et al., 1981]. Point by point check of the leakage current density at low electric fields indicated its value to be less than $2.8x10^{-10}$ A/cm^2 for electric fields up to 1 MV/cm for both as-deposited and annealed nitride films.

The average destructive breakdown electric field, E_{DB}, for these dielectric films obtained from the ramp I-V measurements is given in Table 3.1. A negative gate bias with a ramp rate of 0.5 V/s was used. Approximately 40 MNS structures were used for this measurement and the histogram of breakdown electric fields is shown in Fig. 3.5. Very few number of early failures (< 5 MV/cm) were observed in both these films. The average E_{DB} values for the as-deposited and annealed films are 7.8 and 7.1 MV/cm, respectively. The wide variation of the breakdown fields indicates that these might not be intrinsic in nature but caused by pinhole defects and/or weak spots. At the same time, the average value of 7.1 MV/cm obtained for the annealed films sets a lower limit for the value of the breakdown field of these nitride films.

3.4 Summary and Conclusions

In conclusion, high quality silicon nitride films have been deposited by PECVD using disilane and ammonia diluted in large amounts of helium. A simple process scheme of 250 °C deposition and 400 °C PMA resulted in films with electrical properties comparable, and in some cases superior, to those of films deposited with higher thermal budget processes and/or utilizing additional process steps. The net charge density of the annealed films is ~3 X 10^{11} cm^{-2} with interface trap density in the range of 2-3 X 10^{11} cm^{-2}eV^{-1}. No negative charge trapping was evident from the C-V curves for the annealed structures. We believe that the process gases used combined with the low deposition

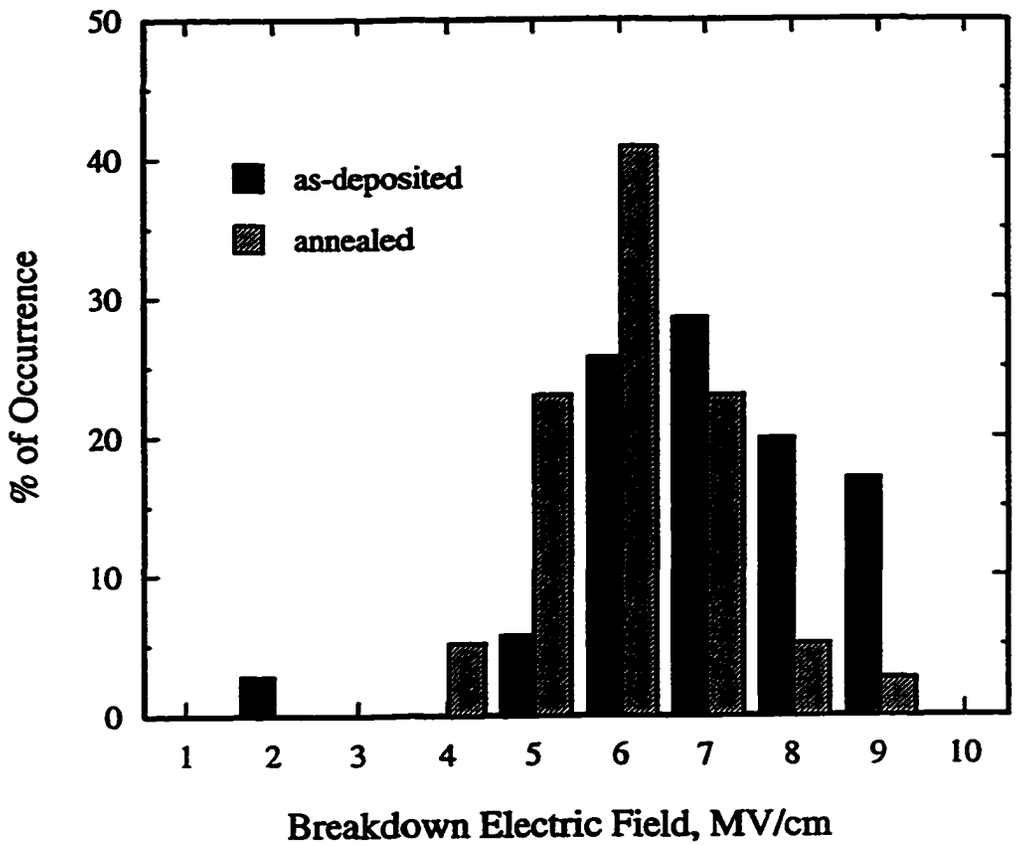


Fig. 3.5. Histogram of breakdown electric fields of as-deposited and annealed silicon nitride films. About 40 devices were used for this measurement.

rates employed are instrumental in obtaining these superior electrical properties. The low thermal budget process scheme utilized in this work makes these silicon nitride films a very viable choice for application in amorphous and poly-Si thin film transistors.

CHAPTER 4. EFFECTS OF PRE- AND POST-DEPOSITION PROCESSING ON ELECTRICAL PROPERTIES

4.1 Introduction

It is well known that the electrical properties of as-deposited dielectric films such as silicon oxide and silicon nitride can be changed by employing different kinds of pre-deposition and post-deposition processing conditions. Some of these electrical properties include net charge density in the films, the interface state density, and leakage current at low electric fields. Thermally grown silicon oxide films exhibit far superior electrical properties upon 30 minute post metallization anneal (PMA) at 400-450 ^{0}C in forming gas (5% H_2 in N_2) ambient [Nicollian and Brews, 1982]. Post-deposition high temperature (>700 ^{0}C) anneal in N_2 ambient is also found to result in improved electrical integrity of these dielectric films.

Low temperature as-deposited PECVD silicon nitride films have high charge density (usually net positive), high carrier trapping rates, high interface state density, and high leakage currents. High temperature (>450 ^{0}C) annealing of these films is usually avoided as it has been found that this results in breaking of Si-H and N-H bonds in the films with accompanied evolution of H_2 [Nguyen 1986]. Typically, annealing temperatures higher than 900 ^{0}C are needed to ensure that this bond breaking is accompanied by new bond formation so that the dangling bond density in the films is low [Lu et al., 1995]. Hence, any annealing process that is compatible with low temperature dielectric process has to be carried out at less than 450 ^{0}C.

Another technique that is employed to achieve better electrical properties for PECVD silicon nitride films is pre-deposition surface treatment. Cleaned substrate surfaces are exposed to plasma generated hydrogen [Arai et al., 1988], oxygen [Lu et al., 1995], and/or nitrogen [Yasui et al., 1994] source radicals. Some of the gases used for this purpose are H_2, N_2O, N_2 and NH_3. These source radicals are expected to be responsible for tying up the surface dangling bonds resulting in low interface state densities. Another means of realizing better electrical properties has been to use stacked dielectrics, especially nitride-oxide (N-O) or oxide-nitride-oxide (O-N-O) layers [Lu et al., 1995]. Although different procedures have been employed by different groups, no systematic comparison of these techniques and their effect on the various electrical properties of the dielectric films exists.

In this chapter, the electrical properties of silicon nitride films subjected to various pre-deposition and post-deposition processing conditions are compared. The different process conditions examined are:

1) Surface treatment by exposure to N_2O plasma

2) Formation of thin (4 nm) silicon oxide as the interface for the nitride films

3) PMA at 420 ^{0}C in N_2 and/or forming gas (FG) ambients.

4.2 Experiment

Chemically polished 4 inch diameter boron doped Si wafers with 100 orientation and 5-10 Ω-cm resistivity were used as the substrates. The process gases for the deposition of these silicon nitride films were 1 sccm of 5% Si_2H_6 in He, 20 sccm of NH_3, and 500 sccm of He. The process gases for the deposition of the thin silicon oxide interface layer were 1 sccm of Si_2H_6 in He, 50 sccm of N_2O, and 500 sccm of He. The

process pressure and rf power for all depositions were maintained at 750 mTorr and 50 W respectively. The substrate temperature was 250 ^{0}C. All the films deposited were of 100 nm thickness. The effective nitirde thickness of the films with the thin oxide interface is calculated from the following equation:

Effective thickness = nitride film thickness + ($\varepsilon_{nit}/\varepsilon_{ox}$) oxide film thickness

where ε_{nit} and ε_{ox} are the relative dielectric constants of PECVD nitride and oxide films respectively. It was assumed in this calculation that the dielectric constant of the thin oxide films is the same as that of thick (100 nm) oxide films.

The conventional RCA cleaning followed by 1 minute dip in 100 : 1 (by volume) of DI water : HF (48%) solution was used as pre-deposition cleaning procedure. The plasma chamber was pumped down to $1x10^{-5}$ Torr base pressure using a oil-free turbo molecular pump after loading the samples and before commencing the deposition process. A chamber pump-down step was introduced between oxide and nitride deposition for the appropriate samples to pump out all the processing gases of the first deposition prior to the second deposition. The thickness of the nitride films was determined by ellipsometry. The individual film thickness values, obtained from extrapolation of film thickness vs deposition time curves, were used to determine the effective nitride thickness of the oxide-nitride composite dielectric layers. All the nitride films were N-rich with no Si-H bonding that could be detected through infrared spectroscopy. Thermally evaporated Al was used as the gate material for the metal-insulator-semicoductor (MIS) capacitors. Standard photolithography technique was employed in preparing these capacitors with a gate area of $2.3x10^{-3}$ cm^2. Aluminum was

evaporated on the back side of the wafer to ensure proper contact. PMA was performed in nitrogen and forming gas ambients at 420 ^{0}C. The annealing time for samples annealed in either N_2 or forming gas ambient was 30 minutes, while a 40 minute anneal with 20 min anneal in N_2 followed by 20 min anneal in forming gas ambient was used for the samples annealed in both ambients.

C-V and I-V curves were acquired as explained in sections 3.2 and 3.3. High-Low frequency capacitance method was used in determining the interface trap density [Castagne and Vapaille, 1971]. The charge trapping behavior of these dielectric films when used in MIS structures was measured at room temperature by observing the flatband voltage (V_{FB}) shift, ΔV_{FB}, of the MIS capacitors with time as a result of either positive or negative stress on the gate terminal. A gate voltage magnitude of 10 V was used for positive and negative gate stressing resulting in stress fields of +1.1 and -0.94 MV/cm, respectively. The average stress field is calculated form $(V_g-\phi_{MS}-\psi_{Si})/t_{ins}$, where V_g is the applied gate voltage, $q\phi_{MS}$ is metal to semiconductor work function difference (-0.88 eV in this work), ψ_{Si} is the potential drop in Si, and t_{ins} is the effective thickness of the insulator film. A fresh capacitor was used for each data point. A stressing time of up to 10 minutes was used to generate the charge trapping curves. The post-stress V_{FB} was measured with a gate voltage scan over 1V range within 3 s of removing the stress voltage. This is important so as to reduce or avoid dissipation of the trapped charges in the films prior to the V_{FB} measurement.

4.3 Results and Discussion

Table 4.1 lists the initial flatband voltage, V_{FBi}, the hysteresis voltage, V_H, interface trap density D_{it} at 0.4 eV above the valence band edge E_V, and the leakage current at negative gate field of 0.94 MV/cm for the MIS capacitors subjected to three different PMA conditions. As described in chapter 3, V_{FBi} is the flatband voltage obtained from the C-V curve plotted for a small range of gate voltage around the flatband voltage. This is done so as not to trap any significant number of carriers during the measurement. A gate voltage sweep from -12 to +8 V was used to generate the 'sweep-right' C-V curves and from +8 to -12 V for the 'sweep-left' C-V curves. The difference between the V_{FB} values obtained from these two C-V curves is the hysteresis voltage, V_H.

The flatband voltage, which is about the same for N_2 and forming gas annealed films was found to be the lowest for films annealed first in N_2 and later in forming gas ambient. This means that the net effective bulk and interface charge density is the lowest for these films. It is calculated to be $2.7 \times 10^{11} q\ cm^{-2}$. A positive value of V_H in the observed C-V curves is indicative of charge trapping in the films due to injection at the silicon-silicon nitride interface and is also observed to be the lowest for films annealed in both ambients. The interface state density shows the same trend as the hysteresis voltage. The mid-bandgap interface state density for films annealed in both gas ambients was found to be $6\text{-}7 \times 10^{10}\ cm^{-2}eV^{-1}$. The leakage current through the films at a negative gate field of 0.94 MV/cm is the same for N_2 annealed and both N_2 and forming gas annealed devices, but is almost an order of magnitude higher for forming gas annealed films. This will be discussed in more detail later in the section.

Table 4.1. Initial flatband voltage V_{FBi}, hysteresis voltage V_H, interface trap density D_{it} at (E_V+0.4) eV, and leakage current density at 0.94 MV/cm E field (negative gate bias) for silicon nitride films subjected to PMA in different ambients.

Annealing Ambient	V_{FBi} (V)	V_H (V)	D_{it} ($cm^{-2}eV^{-1}$)	Leakage Current Density at 0.94 MV/cm E Field (A/cm^2)
N_2	-1.8	0.45	$2\text{-}3x10^{11}$	$2.8x10^{-10}$
Forming Gas	-1.83	0.26	$1\text{-}2x10^{11}$	$1.9x10^{-9}$
N_2 followed by Forming Gas	-1.63	0.18	$1x10^{11}$	$2.9x10^{-10}$

In an effort to lower the interface state density and also to understand the carrier conduction process through the nitride layers, silicon nitride films were deposited with thin (4 nm) silicon oxide forming the interface between the substrate and the nitride films. These devices were subjected to both N_2 and forming gas anneals. A conceptual energy band diagram of a MIS structure with this dielectric as the insulator is shown in Fig. 4.1. The energy barrier for both electron and hole injection from the substrate into the dielectric is higher for oxide-Si interface compared to nitride-Si interface [Aminzadeh et al., 1988]. With a thin oxide layer forming the interface, it is expected that the interface characteristics and efficiency of carrier injection across the interface be different from those of the MNS structures.

The 1 MHz C-V curves of the MNOS capacitors are plotted in Fig. 4.2(a). The V_{FBi} value of this capacitor was found to be -3.3 V, which is almost twice as that of MNS devices subjected to the same annealing process. A comparison of sweep-right C-V curves of the MNS and MNOS devices in Fig. 4.2(b) shows a bigger stretch-out of the curve for MNOS capacitors, possibly due to higher interface trap density. Also, the fixed charge density at the oxide-nitride interface could be responsible for the higher V_{FB} values. Ma et al.[1993] compared the flatband voltage and D_{it} characteristics of oxide and O-N-O dielectrics having the same effective thickness and found that the MIS structures with ONO dielectrics had more negative V_{FB} and higher D_{it} values. They attribute the higher D_{it} values to N-atom pileup at the bottom oxide-Si interface that occurs during the nitride layer deposition. They also found that this N-atom pileup does not affect the V_{FB} values, and attributed the more negative flatband voltages in ONO devices to the charges trapped in the nitride layer and/or the two internal O/N interfaces.

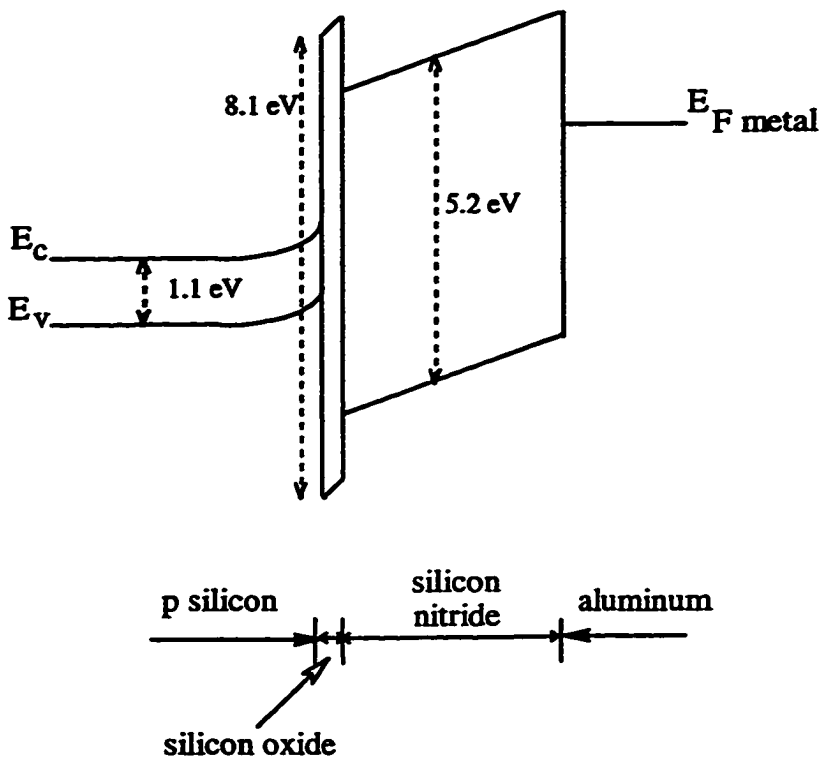
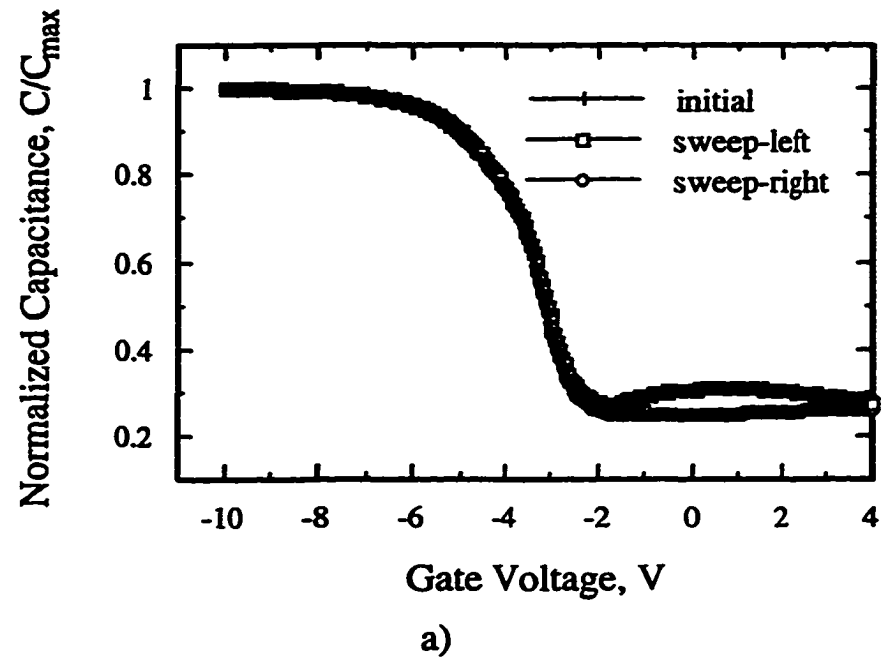
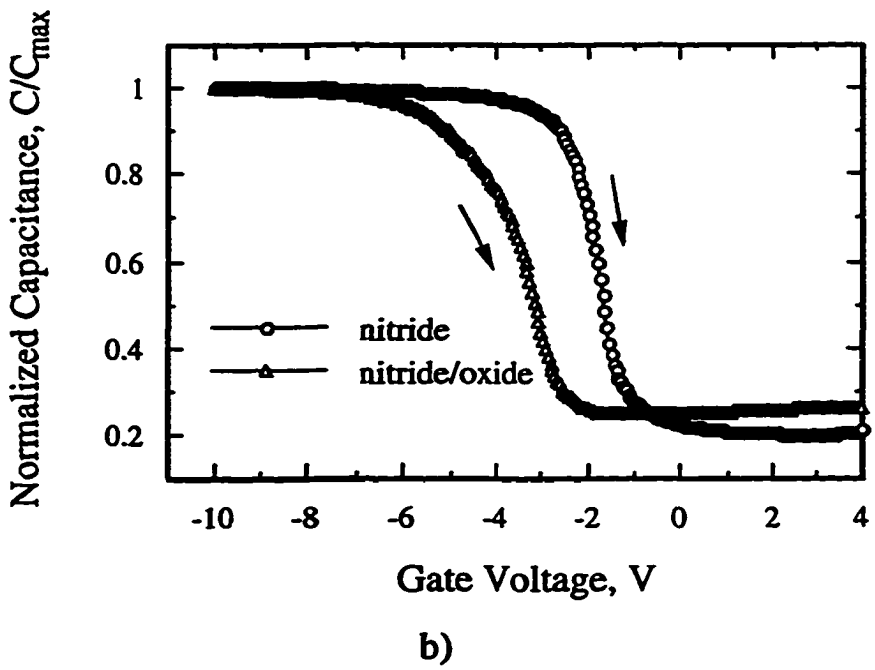


Fig. 4.1. A conceptual energy band diagram of metal-nitride-oxide-semiconductor structure under negative gate bias.



a)



b)

Fig. 4.2. C-V curves for a) MNOS and b) MNS and MNOS capacitors. Sweep-right curves are plotted in b).

Since the oxide interface layer is really thin in this work and also because the same deposition conditions are used for the nitride layer deposition in both the MNS and the MNOS devices, the higher V_{FB} values for the MNOS capacitors are likely due to the charges at the O-N interface. Higher VFB values were also obtained in films for which the substrate received a N_2O plasma surface-treatment prior to the nitride deposition and films deposited on native silicon oxide. Another interesting feature of Fig. 4.2(a) is the lack of hysteresis in the C-V curves which means that the charge trapping in these films is less compared with that in nitride films. This is also evident from trapping studies performed on these devices, presented later in the section.

Fig. 4.3 compares the interface state density of the MNS and MNOS devices subjected to both N_2 and forming gas anneal. The mid-bandgap range D_{it} for the MNOS devices is higher than that for the MNS devices although these values are not higher than the D_{it} values for MNS devices subjected to just N_2 anneal. The ramp I-V characteristics of the MNS devices annealed in the previously stated three different ambients and the MNOS devices that received both N_2 and forming gas anneal are shown in Fig. 4.4. The gate field is negative corresponding to carrier accumulation at the p-type substrate surface and the gate voltage is ramped at a rate of 0.25 V/s. The three MNS devices showed similar characteristics with the nitride films annealed only in forming gas ambient showing higher leakage currents at low applied electric fields and the nitride films annealed in both N_2 and FG showed higher gate current at higher applied electric fields. The ramp I-V curve of the MNOS device looks similar to that of MOS device with Fowler-Nordheim (F-N) type carrier conduction, only that the current

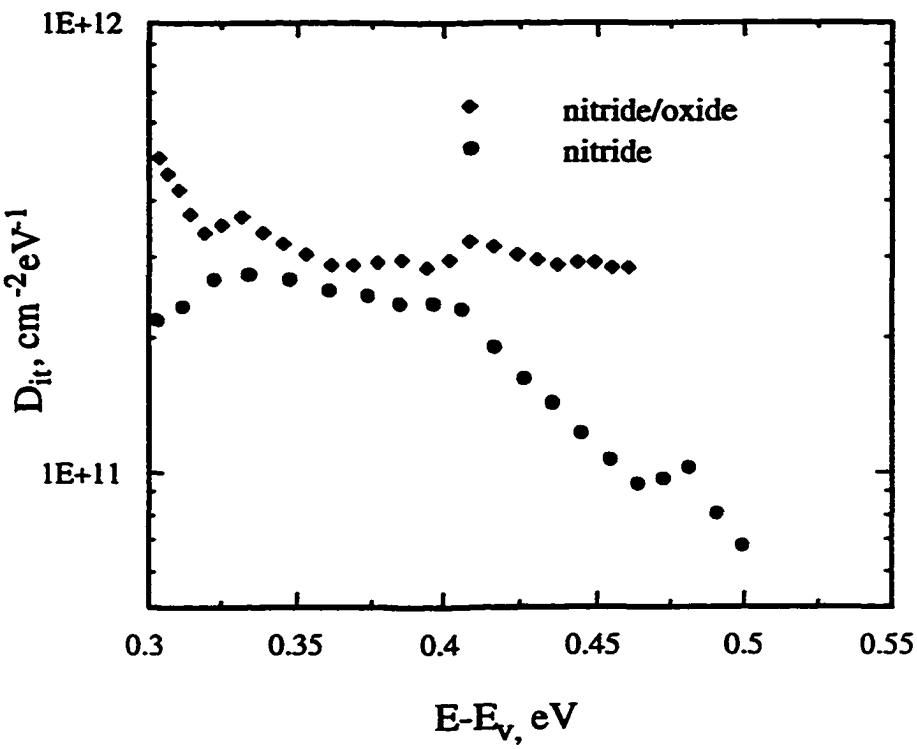


Fig. 4.3. Interface trap density vs position in the silicon bandgap for MIS capacitor with nitride and nitride/oxide dielectrics subjected to both N_2 and forming gas anneal.

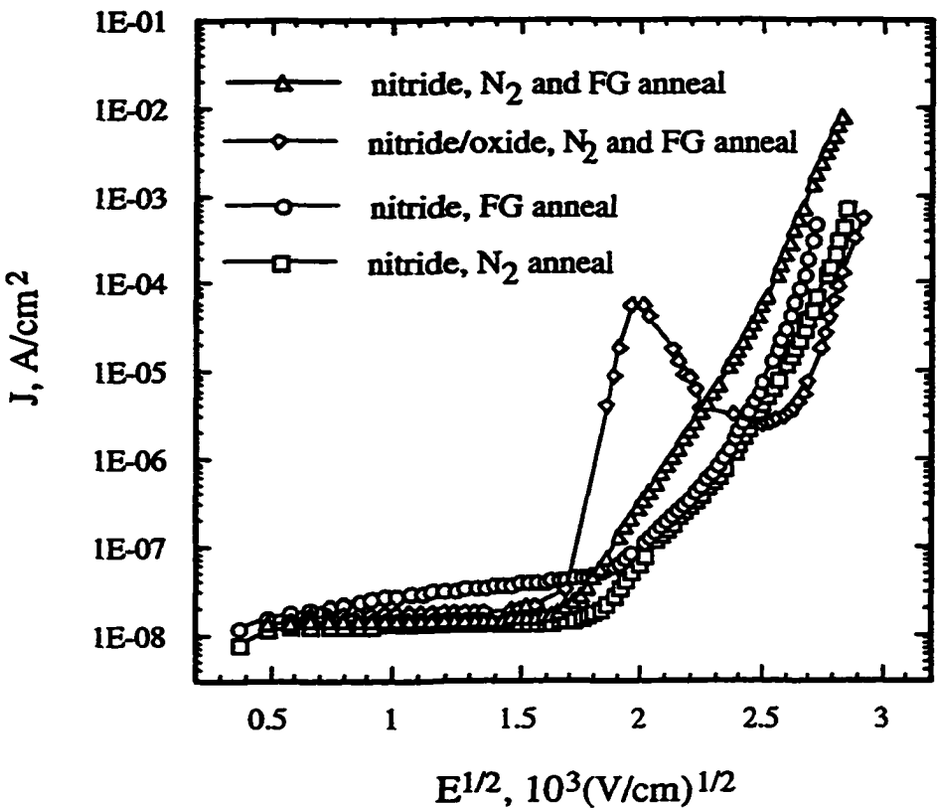


Fig. 4.4. Current density as a function of average electric field obtained by ramp I-V measurements on MNS and MNOS capacitors annealed in different conditions. The ramp rate was 0.25 V/s with gate voltage negative with respect to the substrate.

decreases with increasing E field in the part of the curve where a trapping ledge is usually observed in the I-V plots of devices with F-N tunneling as the dominant current conduction mechanism. No model is available at this time to explain this behavior. For fields higher than 6 MV/cm, all the curves have slopes indicative of Poole-Frenkel emission current conduction mechanism.

The leakage current through these films obtained from point-by-point I-V measurements are plotted in Fig. 4.5 as a function of the applied electric field. As evident from ramp I-V curves in Fig. 4.4, the MNS devices that received only forming gas anneal have much higher leakage current. In fact, the leakage current through these devices is almost two orders of magnitudes higher than that for the MNS devices annealed in both N_2 and forming gas ambients. The leakage current values for the MNOS devices are in between that for the two different MNS devices. It has long been believed that holes are the dominant conduction carriers in PECVD nitride films [Weinberg and Pollak, 1975]. Considering this, it is not understood why the presence of the thin oxide, which provides higher barrier for hole injection from Si substrates under negative gate bias (refer to Fig. 4.1), does not result in low leakage currents at low E fields.

The V_{FB} shift (given by V_{FB} (after stress) – V_{FB} (initial)) with time under constant E field stressing of the MNS devices annealed only in forming gas ambient and in both N_2 and forming gas ambients is plotted in Fig. 4.6. Figure 4.6(a) is plotted for negative stress voltages at the gate with Fig. 4.6(b) plotted for positive stress voltages. The V_{FB} shift under negative voltage stress exhibits logarithmic relation with stress time. This behavior is more so for the films annealed in both N_2 and forming gas

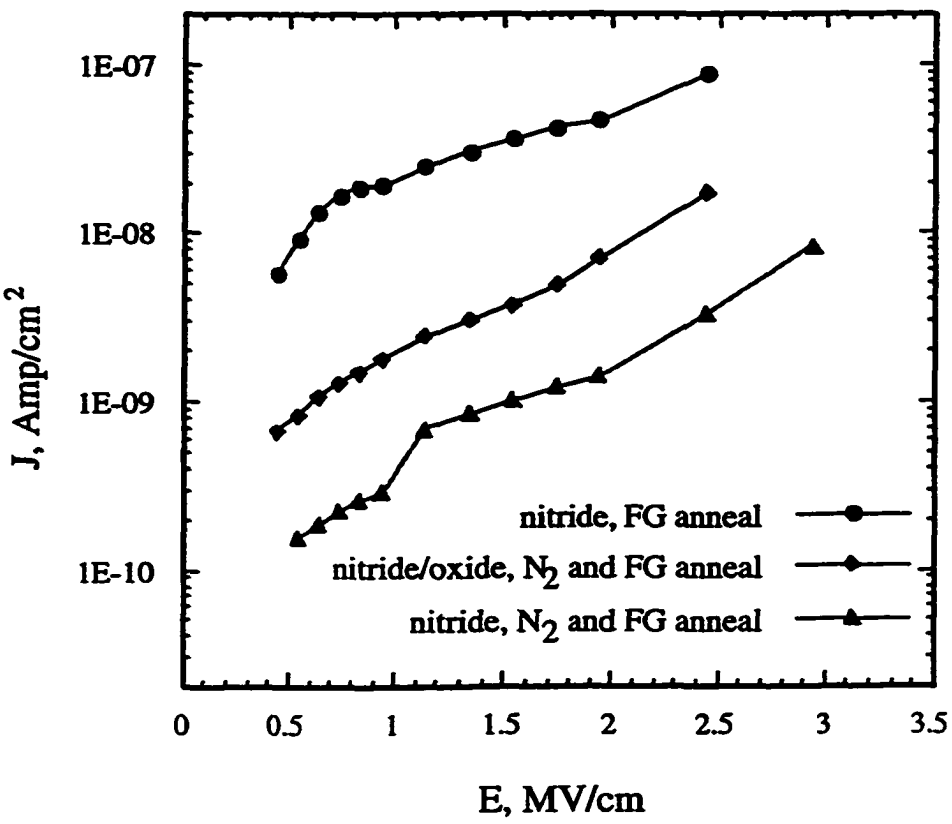
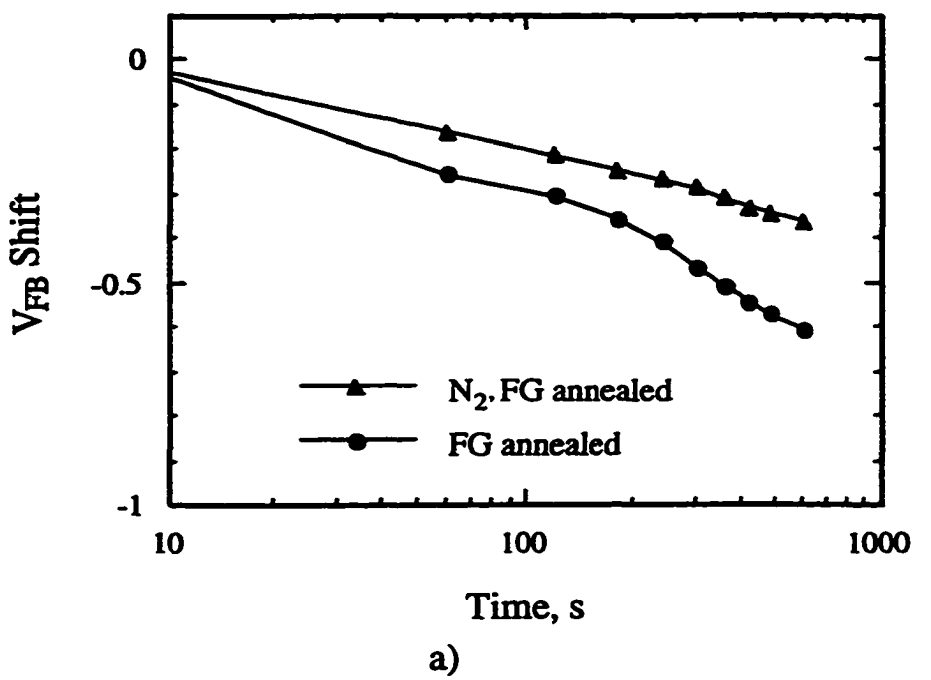
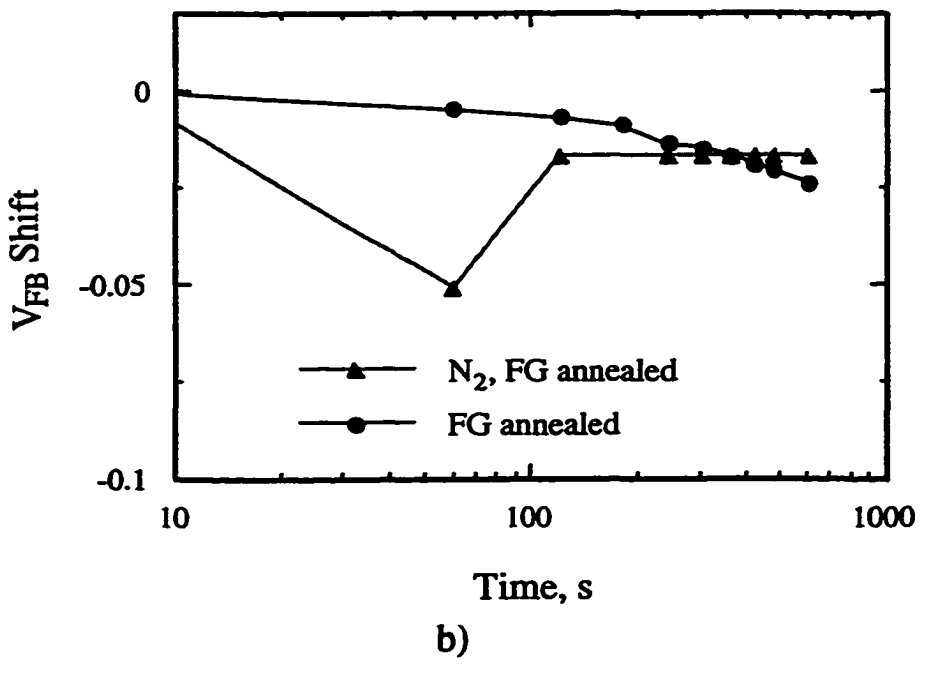


Fig. 4.5. Leakage current density through nitride and nitride/oxide dielectric films annealed in different conditions plotted as a function of the applied average electric field.



a)



b)

Fig. 4.6. Flatband voltage shift vs time for MNS capacitors annealed in different conditions; a) gate voltage negative with stress field of 1.1 MV/cm; b) gate voltage positive with stress field of 0.92 MV/cm.

ambients. The direction of V_{FB} shift indicates net positive charge trapping in the films. This might be due to the holes injected from the hole accumulation layer at the p-type Si surface that exists under negative gate voltages. Though electron injection from the gate is possible, the effect of this charge layer on the V_{FB} shift of the device would be considerably less than that of the trapped holes close to the Si-silicon nitride interface.

From Fig. 4.6(a), we see that the magnitude of the V_{FB} shift is smaller for devices annealed in both N_2 and forming gas ambients indicating smaller trap density close to the interface in these films. An E field of 0.94 MV/cm is probably not high enough to fill the traps well into the bulk of the nitride film from the Si surface. The V_{FB} shift after 10 minute stress was -0.35 V for films annealed in both gas ambients whereas this value was -0.62 V for films annealed only in forming gas. Neither of these films exhibits any significant V_{FB} shift under positive gate voltage stress, as is seen from Fig. 4.6(b). This indicates that there is little electron trapping in these nitride films. In fact, the slightly more negative V_{FB} values for the stressed films could be due to the trapped hole charge at the metal-nitride interface and/or ion motion in the nitride film.

Figure 4.7 compares the V_{FB} shift for MNS and MNOS devices for negative gate voltage stress. Both MNS and MNOS devices in this plot received N_2 and forming gas anneals. The MNOS devices exhibit a positive V_{FB} shift for negative gate voltage stress. This shows that there is net negative charge trapping in the films with the trapped charge injected from the gate in the form of electrons and/or ion motion in the nitride film towards metal-nitride interface. The absence of hole trapping is according to expectations, since the thin interfacial oxide layer offers a higher barrier to hole

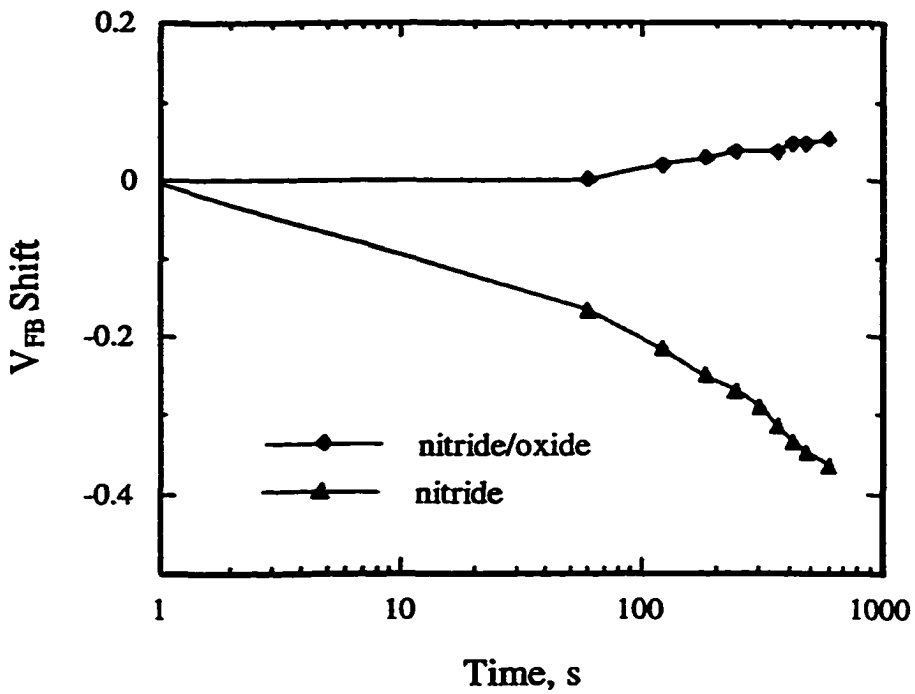


Fig. 4.7. Flatband voltage shift vs time for MNS and MNOS capacitors under negative gate voltage stress. The stress field was 0.94 MV/cm. Devices were annealed in N_2 and forming gas.

injection from the Si surface into the dielectric film. This may also explain the lack of hysteresis in the C-V curves in Fig. 4.2(a).

4.4 Summary and Conclusions

The influence of PMA in different ambients on the electrical properties of silicon nitride films examined in chapter 3 is studied. Films were subjected to N_2 anneal, forming gas anneal, and both N_2 and forming gas anneal at 420 ^{0}C. The electrical properties of silicon nitride films deposited after the formation of thin plasma deposited silicon oxide as the interface are also studied.

Silicon nitride films subjected to both N_2 and forming gas anneal were found to have superior electrical properties to those of films annealed in either N_2 or forming gas ambients alone. The net bulk and interface charge density, charge trap density, D_{it} in the mid-bandgap region, and leakage current through the films were all lower for films annealed in both N_2 and forming gas ambients. The leakage current density for these 100 nm thick films was less than $5x10^{-10}$ A/cm^2 for gate voltages up to 12 V and less than $5x10^{-9}$ A/cm^2 up to gate voltages of 25 V. This means that these films of 100 nm thickness are more than adequate as dielectrics in TFT structures where the typical voltages encountered are less than 10 V. Dielectric films with higher leakage currents and accompanied charge trapping, when used as insulators in MISFETs, are responsible for time-varying device characteristics. The films studied here, with very low leakage currents and charge trapping properties that are not intolerable, seem to be a very viable choice as gate dielectrics in TFTs.

MNOS devices with ~4 nm thick silicon oxide layer forming the interface with the Si substrate were found to have larger values of V_{FB} than the MNS devices. The

other properties examined were similar to those of the nitride films annealed in both N_2 and forming gas ambients, with the exception of charge trapping properties which are far superior for nitride-oxide films. This is believed to be due to the higher barrier at the Si-silicon oxide interface to hole injection from the Si surface. With the aid of this structure, it was also deduced that hole trapping is the dominant trapping mechanism in these nitride films.

CHAPTER 5. SILICON OXYNITRIDE FILMS

5.1 Introduction

It has been known that converting a plasma silicon nitride film to silicon oxynitride film by introducing oxygen improves the film's thermal stability, cracking resistance, and decreases stress in the film [Nguyen 1984]. It also has been reported that oxynitride films with oxygen concentration of around 16-20 atomic % appears to have better physical and electrical properties compared to nitride and other oxynitride films [Nguyen 1986]. Silicon oxynitride film properties can be easily modified by varying the film composition through deposition conditions. For these reasons, oxynitride thin films have found many applications such as 1) final passivation layers in IC devices, 2) inter-metal dielectric layers, 3) charge storage material in memory devices [Shams and Brown, 1990], and more recently as 4) the gate insulator in TFT technology [Cros et al., 1992]`. The reduced stress in oxynitride films makes them an attractive choice as gate dielectrics in TFTs, since films in active matrix liquid crystal display (AMLCD) manufacturing process need to be deposited over large area glass substrates with good uniformity and little stress.

In this chapter, the process details for the deposition of silicon oxynitride films, by introducing N_2O as the oxygen source into the silicon nitride deposition process with disilane, ammonia, and helium, are presented. The electrical properties of these films deposited under varying flow rate ratios of NH_3 and N_2O are examined in detail and compared to those of silicon nitride films presented in chapters 3 and 4. The suitability

and advantages of these films as gate dielectrics in TFT manufacturing process is addressed.

5.2 Experiment

Chemically polished 4 inch diameter boron doped Si wafers with 100 orientation and 5-10 Ω-cm resistivity were used as the substrates. The wafers were cleaned as per the standard RCA cleaning procedure and were dipped in 100 : 1 (by volume) of DI water : 48% HF for 1 minute to strip the native oxide. The chamber was pumped down to a base pressure of $1x10^{-5}$ Torr by turbomolecular pump after loading the samples and before commencing the deposition process. The oil-free environment reduces surface contamination prior to film deposition. Silicon oxynitride films were deposited by flowing 20 sccm of 1% disilane in helium, 20 sccm of ammonia, 500 sccm of helium, and 0-10 sccm of nitrous oxide into the deposition chamber and subjecting to plasma excitation. The N_2O flow rate is the only process parameter varied in this experiment resulting in flow rate ratio of N_2O to NH_3 from 0 to 0.5. The process pressure and rf input power were maintained at 750 mTorr and 50 W respectively. The substrate temperature was 250 ^{0}C with the upper electrode at 60 ^{0}C.

The thickness and refractive index of these films were measured using an ellipsometer. The Fourier transform infrared (FTIR) spectra of the films were obtained with a Perkin-Elmer model 1600 FTIR spectrophotometer. A bare Si wafer was used as the background reference. Thermally evaporated aluminum was used as the gate metal and standard photolithography was used in defining MIS capacitors with gate area of 0.0023 cm^2. All the oxynitride films used in electrical characterization were of 100 nm thickness as determined by ellipsometry. The PMA was carried out at 420 ^{0}C for 20

minutes in N_2 gas followed by 20 min in forming gas ambient. The high frequency C-V measurements were carried out by superimposing a 20 mV ac signal of 1MHz frequency on a dc ramp voltage with a ramp rate of 0.02 V/s. The trace and re-trace of the C-V curves were done between gate voltage interval of $-(10+|V_{FB}|)$ and $+(10+V_{FB})$ V. The gate voltage was maintained constant at the beginning of each scan for 35 s at the extreme bias value to approach a steady state. The low-frequency (LF) C-V curves were generated using charge-voltage method with gate voltage steps of 20 mV and step delay time of 5 s. High-Low frequency capacitance method was used in estimating the D_{it} values for these films. The I-V characteristics were obtained using a ramp gate voltage with ramp rate of 0.25 V/s. A staircase shaped gate voltage was used in point-by-point measurement of leakage current through these films. The procedure for measuring the V_{FB} shift on constant gate voltage stressing of the capacitors is the same as explained in section 4.2.

5.3 Results and Discussion

The deposition rate and refractive index n of the silicon oxynitride films are plotted as a function of flow rate ratio of N_2O to NH_3 in Fig. 5.1. The N_2O flow rate was varied from 0 to 10 sccm with the flow rate of ammonia fixed at 20 sccm. The deposition rate increases with increasing N_2O flow due to the lesser excitation energy of N_2O molecule compared with NH_3 molecule. Since, disilane molecule has the lowest dissociation energy of the three source molecules in the plasma, it is expected that the film interface is Si-rich with a gradual transformation to weakly nitrided silicon oxide and eventually to silicon oxynitride layers. Nguyen [1986] reported that this interfacial layer could be as thick as 10-20 nm. It is also possible that the interfacial layer thickness

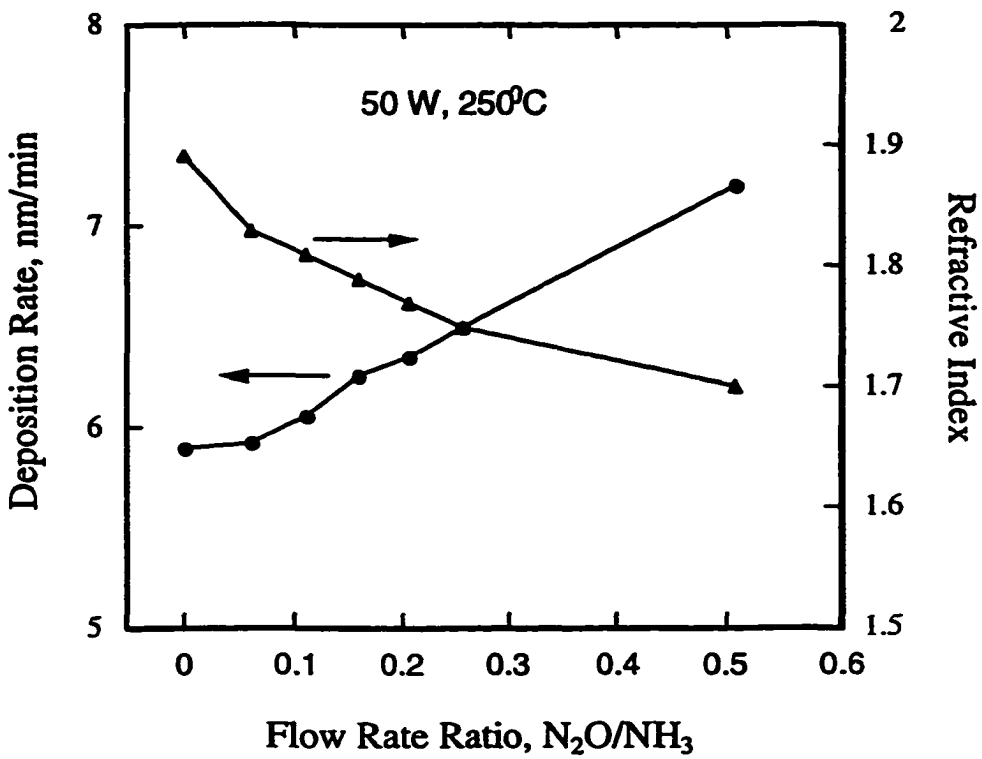


Fig. 5.1. Deposition rate and refractive index of silicon oxynitride films as a function of flow rate ratio of N_2O to NH_3. Process pressure is 750 mTorr and flow rates of NH_3, Si_2H_6 and He are fixed at 20, 1, 500 sccm respectively.

is dependent on the N_2O flow rate, since this changes the concentration of source radicals available for the formation of silicon oxide or weakly nitrided silicon oxide during the initial phases of the plasma deposition process. The refractive index of the films decreases with increasing N_2O flow indicating incorporation of more and more O atoms into the deposited film. The refractive index value starting at 1.9 for O-free films decreases with increasing N_2O flow rate and is 1.7 for films deposited with 10 sccm N_2O flow.

The FTIR transmission spectra of these films are shown in Fig. 5.2. None of the films exhibit the Si-H stretching mode peak at 2160 cm^{-1}. The are two notable features in this plot. First, the shifting of the peak position of the broad absorption band that is centered around 870 cm^{-1} for silicon nitride films. This peak gradually shifts towards higher wave numbers with increasing N_2O flow rates. This is another indication of increasing O concentration (Si-O bond concentration, to be exact) in the films, since the Si-O absorption band is centered around 1070 cm^{-1}. Secondly, using the integrated area enclosed by the N-H absorption band centered around 3330-3350 cm^{-1} as a measure of the H concentration in the films, it is evident that the latter decreases with increasing O concentration. Since silicon oxide films deposited in the same reactor at 250 ^0C did not show significant Si-OH bond concentration [Song et al., 1995], the H content bonded to O atoms in these oxynitride films was considered negligible compared to the H concentration bonded to N atoms.

The effect of O incorporation into the nitride films on their electrical properties is discussed below.

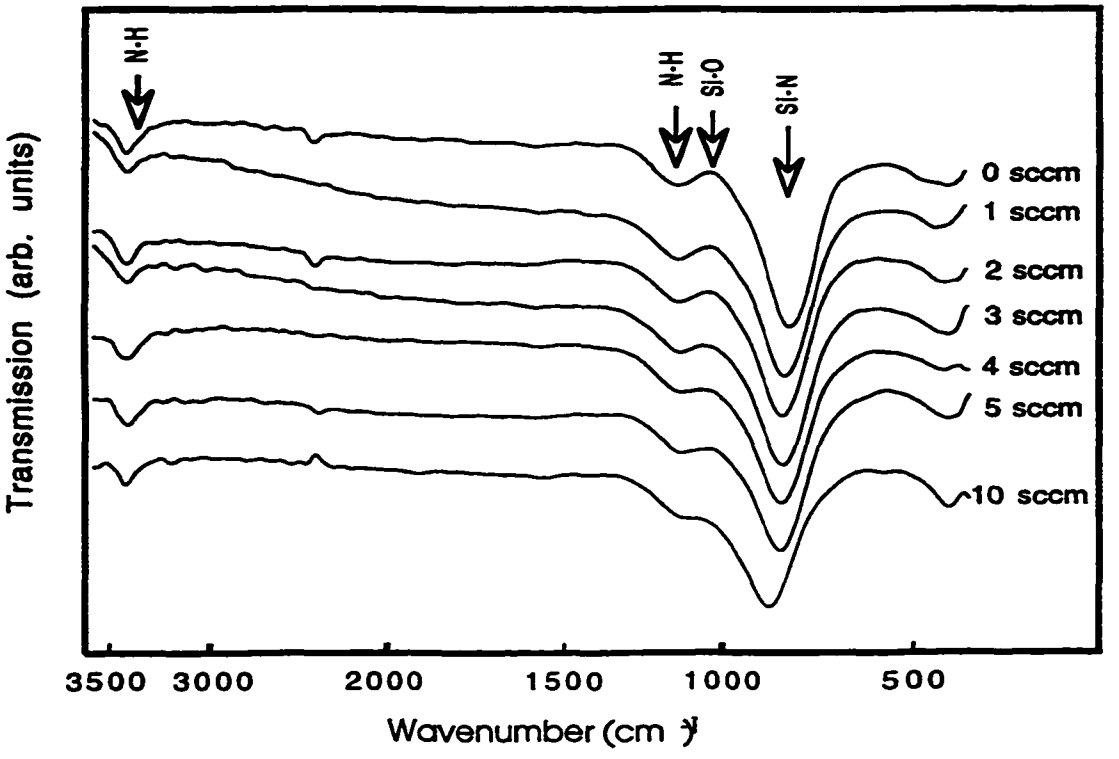


Fig. 5.2. Infrared transmission spectra of silicon oxynitride films with varying nitrous oxide flow rates. Flow rates of ammonia, disilane, and helium were fixed at 20, 1, and 500 sccm respectively. rf power = 50 W, process pressure = 750 mTorr and deposition temperature = 250 ^{0}C. The plots are vertically offset for clarity.

Fig. 5.3 shows the high-frequency (HF) C-V curves of the oxynitride films deposited with varying N_2O flow rates. As seen from the figure, the curves shift toward more negative gate voltages with increasing N_2O flow rate, indicating more negative V_{FB} values and hence increasing net effective positive charge in the films. The stretch-out in the curves remains nearly the same for low N_2O flow rate films, increases at high N_2O flow rates and is largest for films deposited with 10 sccm N_2O flow rate. The increasingly negative values for V_{FB} with increasing O concentration in the films is contrary to the results reported by Ma and Lucovsky [1994] where increasing O content in oxynitride films was found to result in less negative V_{FB} values. These authors employed remote PECVD (RPECVD) process for their film deposition where the nitrogen and oxygen source gases are excited by plasma in a separate chamber and then subsequently mixed with silane in the deposition chamber. This fundamental difference of plasma excitation and source gas mixing between RPECVD and conventional parallel-plate PECVD processes is, in our opinion, believed to be responsible for the opposite trend observed here. In other words, the thin interfacial region that is expected to form during the initial phase of conventional PECVD process, and was discussed before, is believed to be the cause for more negative V_{FB} values for oxynitride films compared to the nitride films. Also, the increasing V_{FB} magnitudes with increasing N_2O flow rates indicates that the defect density of this interfacial layer is possibly higher for higher N_2O flow rates. The higher magnitudes of V_{FB} for MNOS capacitors compared to MNS capacitors, reported in chapter 4, renders support to this observation. The maximum capacitance value in accumulation from the HF C-V measurement was used as the insulator capacitance. This capacitance value was used in determining the 1 MHz

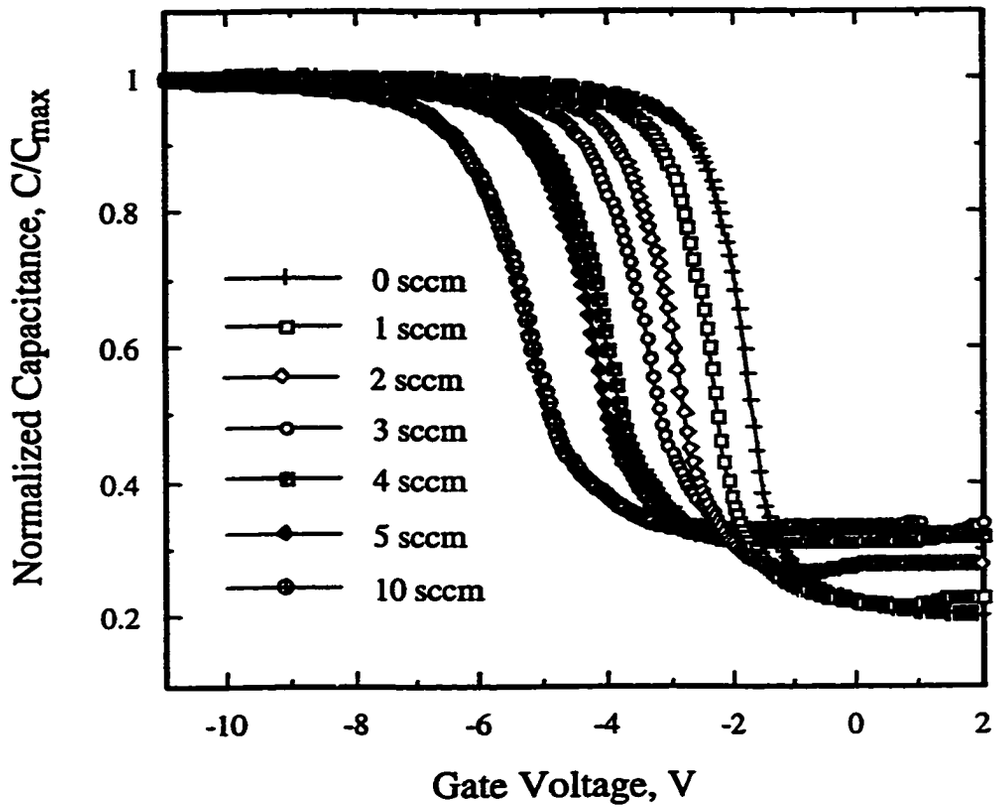


Fig. 5.3. C-V curves at 1 MHz for Metal-Oxynitride-Semiconductor capacitors with the oxynitride layer deposited under different N_2O flow rate conditions. The gate voltage was swept from negative to positive voltage.

static dielectric constant of the films. The relative dielectric constant values for the oxynitride films deposited using various N_2O flow rates are shown in Fig. 5.4.

The values of V_{FB} and their hysteresis V_H from the C-V curves are plotted in Fig. 5.5. The flatband voltage increases from -1.63 V for nitride films (0 sccm N_2O flow) to 5 V for oxynitride films deposited using 10 sccm of N_2O flow. The hysteresis voltage, which is the difference between the flatband voltages obtained from C-V curves generated using different scan directions, initially decreases with increasing N_2O flow rates, but increases for films deposited with 10 sccm N_2O flow. In fact, these films exhibited the highest hysteresis of all the oxynitride films investigated. The interface trap density for these oxynitride films is plotted in Fig. 5.6 as a function of position in the Si bandgap. The D_{it} values are found to be nearly the same with similar profiles for the nitride film and the oxynitride films deposited with small N_2O flow rates with a slight tendency for decrease in D_{it} up to 5 sccm. But the oxynitride films deposited using 10 sccm of N_2O showed D_{it} values that are 2-3 times higher than that for the other films. This behavior is somewhat similar to the one observed for hysteresis in Fig. 5.5. The interface trap density at 0.4 eV from the valence band edge is plotted in Fig. 5.7 for the films deposited with different N_2O flow rates. As mentioned before, the D_{it} values for films deposited tends to decrease slightly up to 5 sccm N_2O flow rate with the 10 sccm N_2O flow giving the highest values. It is not known if this increased interface trap density is linked to the higher hysteresis voltages for these films.

The shift in V_{FB}, given by V_{FB} (post-stress) – V_{FB} (pre-stress), with time under constant negative gate voltage stress at room temperature, is plotted in Fig. 5.8 for the nitride and oxynitride films. A negative value of shift shown in Fig. 5.8 is similar to

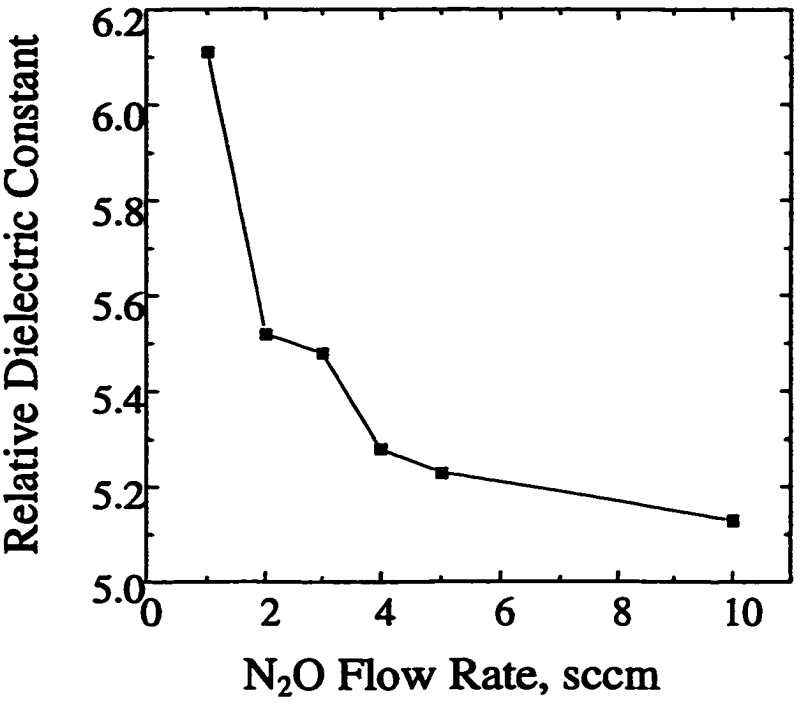


Fig. 5.4. Relative dielectric constant of silicon oxynitride films as a function of the N_2O flow rate. The flow rates of disilane, ammonia and helium were fixed at 1, 20, and 500 sccm respectively.

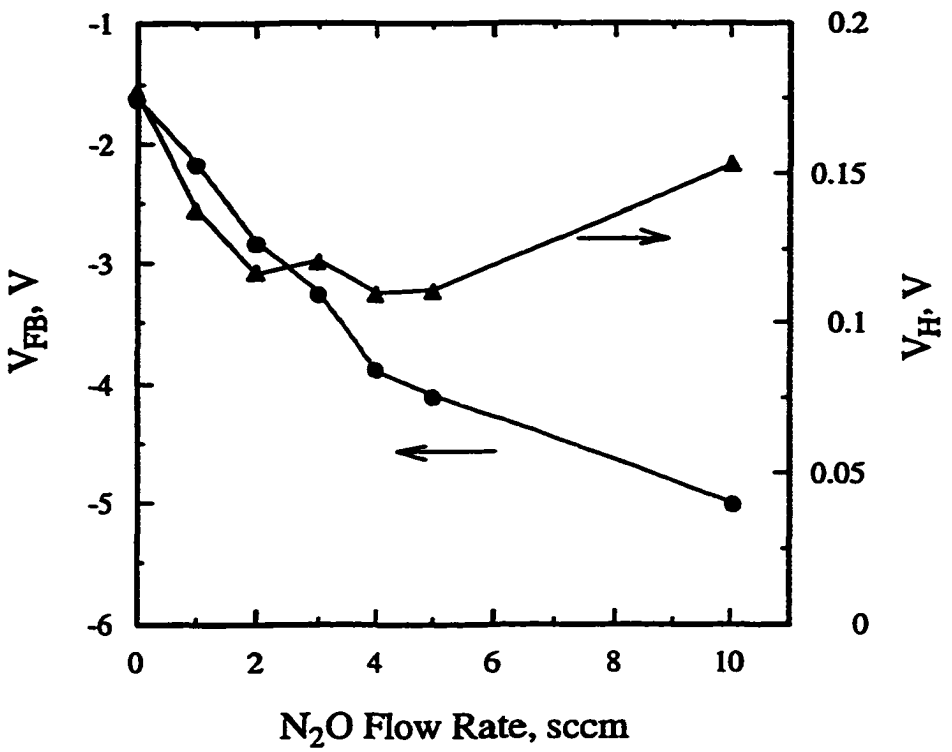


Fig. 5.5. The flatband voltage and hysteresis values for the metal-oxynitride-semiconductor capacitors as a function of N_2O flow rate used for the oxynitride layer deposition.

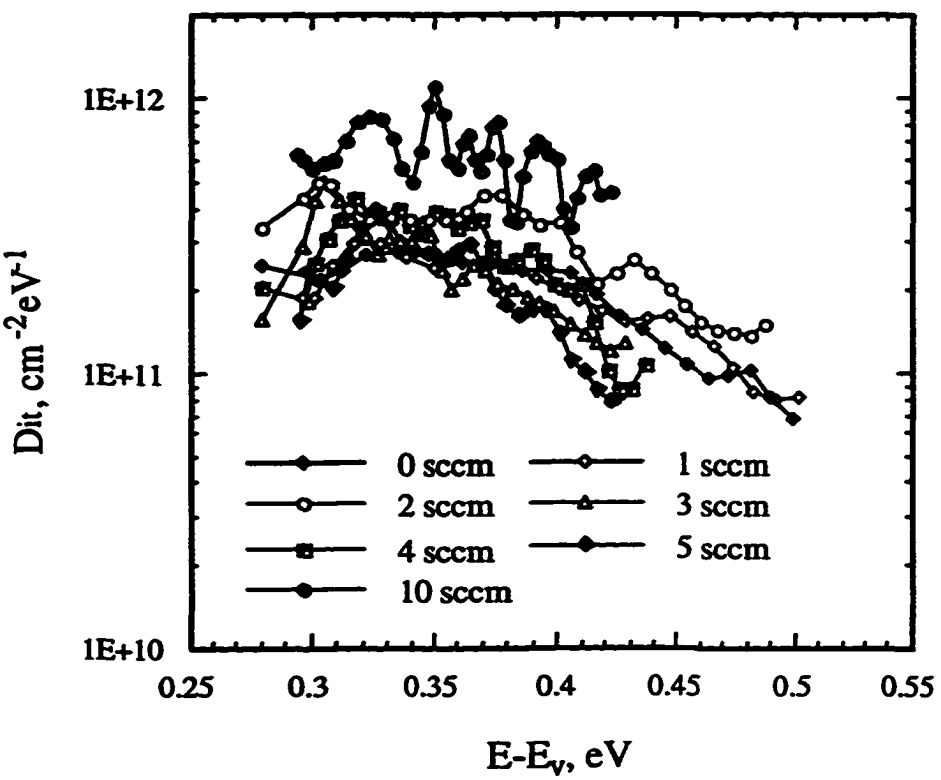


Fig. 5.6. Interface trap density vs position in the silicon bandgap for metal-oxynitride-semiconductor capacitors with the oxynitride films deposited with different N_2O flow rates.

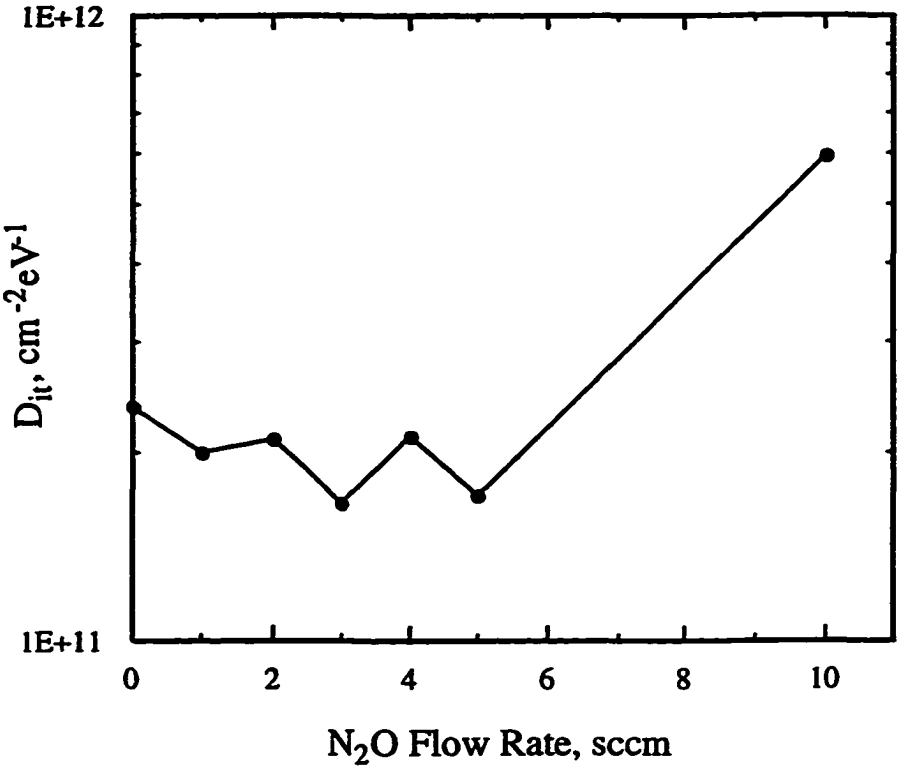


Fig. 5.7. The interface trap density at 0.4 eV above E_V in the silicon bandgap for films deposited with different N_2O flow rate conditions.

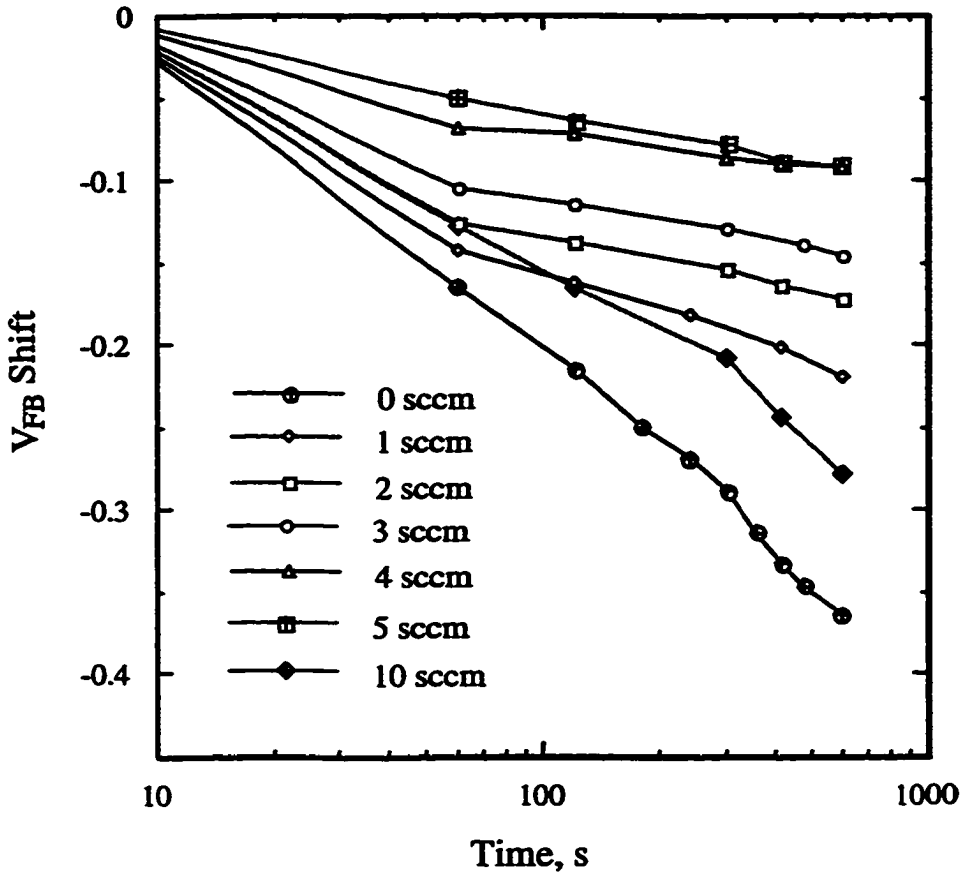


Fig. 5.8. Flatband voltage shift vs bias time for oxynitride layers deposited with different N_2O flow rates. The gate stress voltage was negative and the stress field was 1.1 MV/cm.

instability observed with positive charge injection at the insulator-semiconductor interface. All the curves shown in Fig. 5.8 exhibit logarithmic relation with time. The magnitude of the V_{FB} shift for a certain stress time progressively decreases with increasing N_2O flow rates used for deposition till the flow rate of 5 sccm. This can be attributed to the reduced trap density in the oxynitride films and/or lower hole injection efficiency across the Si-oxynitride interface barrier. The oxynitride films deposited at 10 sccm N_2O have the highest V_{FB} shift among all the oxynitride films. In fact, this trend is similar to the one noticed for the hysteresis voltages, which is not unexpected since hysteresis in C-V curves is related to charge trapping and memory effects.

The V_{FB} shift with time under positive gate voltage stress is plotted in Fig. 5.9. All the films including the nitride films showed very small negative V_{FB} shift which corresponds to net ion motion in the films or net charge injection at the metal-insulator interface. The nitride films showed the smallest shift of the films examined. There was no definite trend among the V_{FB} shift values for the oxynitride films. But all the values seem to be clustered around - 0.05 V for 10 min stress time at 1MV/cm field. The behavior indicated in Fig. 5.9 can result from rapid ion motion through the insulator followed by charge injection and trapping at the semiconductor-insulator interface.

The ramp I-V curves for MIS capacitors with films deposited using N_2O flow rates of 0, 1, 2, 5, and 10 sccm are shown in Fig. 5.10. All the curves except that for films deposited using 10 sccm N_2O flow rate show similar J vs $E^{1/2}$ slope in the high field regime. This slope indicates that the carrier conduction in these dielctric films is by Poole-Frenkel emission [Sze 1969]. The J vs $E^{1/2}$ slope in the high field regime for

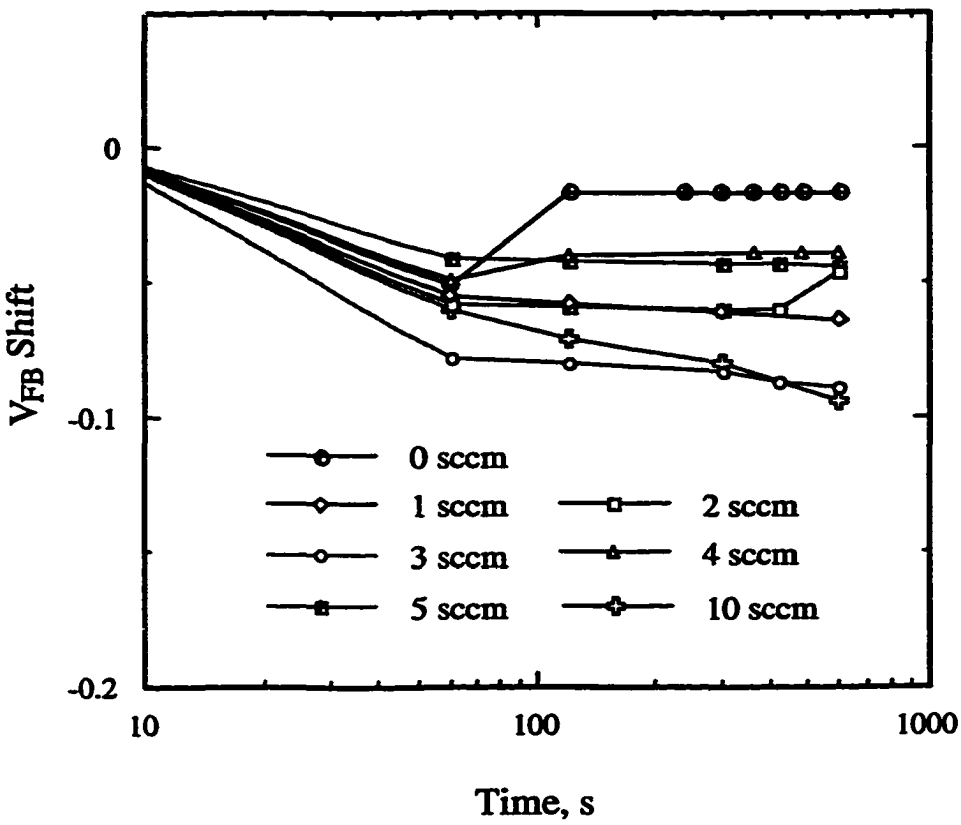


Fig. 5.9. Flatband voltage shift vs time for oxynitride layers deposited with different N_2O flow rates. The gate stress voltage was positive and the stress field was 1.1 MV/cm.

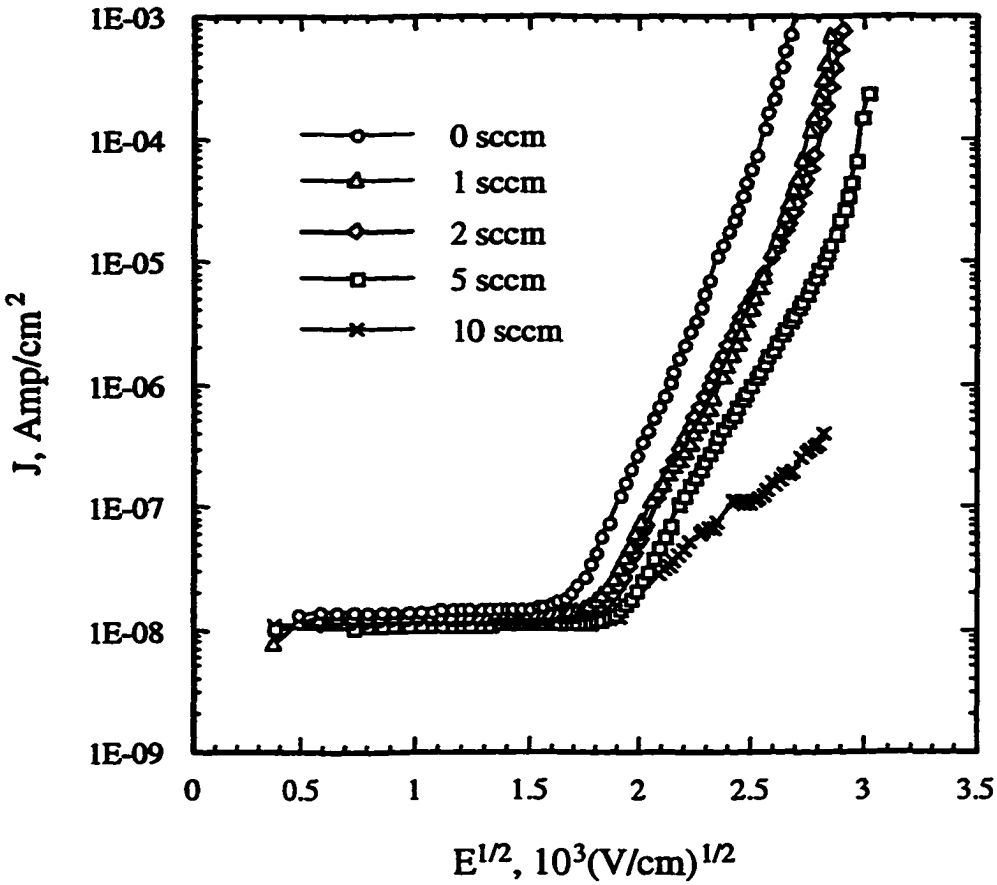


Fig. 5.10. J vs (electric field)$^{1/2}$ curves obtained from ramp I-V measurements for silicon nitride film and oxynitride films deposited with N_2O flow rates of 1, 2, 5, and 10 sccm. The gate voltage was negative with respect to the substrate.

films deposited using 10 sccm N_2O flow rates was much smaller than that for the other oxynitride films. This indicates that the incresing oxygen concentration in the films might be responsible for a change in current conduction mechanism. Pure silicon oxide PECVD films (deposited with no ammonia flow) have been reported to show Fowler-Nordheim type current conduction [Song et al., 1995]. Films deposited with higher N_2O flow rates (until 5 sccm) have the 'knee-portion' of the curves shifted toward higher E fields indicating that the leakage current is lower for films deposited using higher N_2O flow. The I-V curve for the oxynitride films deposited using 10 sccm N_2O flow shows higher leakage current at low electric fields. This, in fact, is evident from Fig. 5.11 where the current through the films obtained from point-by point measurement is plotted for films deposited using 0, 1, 2, and 10 sccm N_2O flow rates as a function of average E field. The leakage current is indeed lower for films deposited with higher N_2O flow rates until flow rate of 2 sccm, with the leakage current in the 3, 4, and 5 sccm instances (not plotted in Fig. 5.11) being very similar to that for films deposited using 2 sccm N_2O flow rate. Films deposited using 10 sccm N_2O flow rate showed, as expected from ramp I-V measurements, the highest leakage current of all the films tested.

Ramp I-V measurements were performed with negative gate voltage and a ramp rate of 0.5 V/s to identify the destructive breakdown voltage of the oxynitride films deposited at N_2O flow rates of 1, 2, and 5 sccm. Approximately 40 capacitors were tested for each dielectric film. It was found that more than 90% of the capacitors with silicon oxynitride films showed dielectric breakdown fields of more than 10 MV/cm.

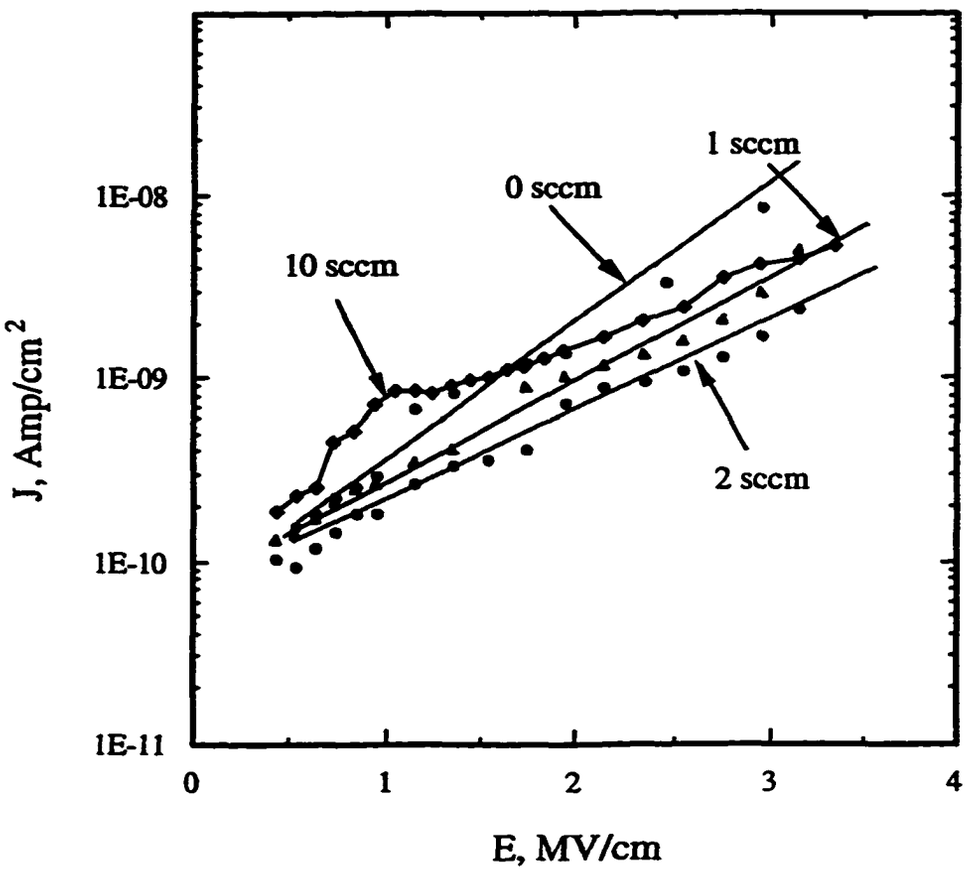


Fig. 5.11. Leakage current through silicon nitride films and oxynitride films deposited with N_2O flow rates of 1, 2, and 10 sccm plotted as a function of the applied gate electric field. The gate voltage is negative with respect to the substrate.

Comparing this to data from Fig. 3.5 for nitride films, it is evident that the extrinsic defect density of the oxynitride films is lower than that for nitride films.

5.4 Summary and Conclusions

Silicon oxynitride films have been deposited by introducing N_2O into the disilane/ammonia/helium gas system that has been used in the earlier chapter for deposition of nitride films. The electrical properties of these films observed from measurements on MIS capacitors incorporating these insulator films are detailed and compared with those of nitride films from the previous chapter. Oxynitride films deposited with higher N_2O flow rates were found to have higher net effective fixed charge density in the films. The instability due to charge trapping in the oxynitride films was found to be less than in nitride films and was lower for films deposited using higher N_2O flow till flow rate of 5 sccm. The carrier conduction mechanism is the same as in nitride films although the leakage current was lower for films deposited with higher N_2O flow rates. Another improvement is fewer number of extrinsic breakdowns of these oxynitride films compared with silicon nitride films consistent with lower pin hole density in oxynitride layers. This could be an important issue in TFT gate dielectric process where films are deposited over large substrate areas and very few defective pixels can be tolerated. Reviewing the overall properties of these films, it was deduced that the silicon oxynitride films deposited using N_2O flow rate of 1 sccm would be the most practical choice for use as gate dielectrics in TFT applications.

CHAPTER 6. SUMMARY

Plasma enhanced chemical vapor deposition of silicon nitride and oxynitride films using disilane as the silicon source is studied. Process characterization details along with the electrical properties of these dielectric films are reported, for the first time, using disilane and ammonia as the process source gases.

The process characterization of deposition of silicon nitride films using disilane as silicon source, ammonia as nitrogen source and helium as diluent gas revealed two regimes of deposition, namely excess-disilane regime and excess-ammonia regime. Films deposited under process conditions falling at the boundary of these two regimes had deposition rates that were mostly dependent on rf power and gas flow ratio resulting in thickness unformity of within ±3% across 4" diameter wafer and highly repeatable film qualities. The large amount of helium dilution utilized in this work resulted in silicon nitride film deposition rates that were less variant with substrate temperature than the reported data for silane based systems. These films were also found to be N-rich with no detectable Si-H bonding in the films. The process window identified in this investigation was used in deposition of silicon nitride and oxynitride films for the purpose of electrical characterization.

Electrical characterization of the silicon nitride films deposited using process conditions falling at the boundary of the above-mentioned regimes showed net positive interface charge density in the films. The films also exhibited instability due to positive charge injection from the Si-substrate under negative gate voltage bias conditions. Net effective interface charge density, instability due to charge injection and the interface

state density of these silicon nitride films all decreased upon post-metalization anneal. Films deposited at 250 ^{0}C and post-metalization annealed in N_2 ambient at 420 ^{0}C exhibited effective fixed interface charge density of ~3x10^{11} cm^{-2} and minimum interface state density of 2-3 x 10^{11} $cm^{-2}eV^{-1}$. Silicon nitride films deposited on native silicon oxide on silicon showed fixed charge density three times higher than that for films deposited on native oxide free surfaces. Both as-deposited and annealed nitride films exhibited leakage current density of less than 2.8 x 10^{-10} A/cm^2 for average electric fields up to 1 MV/cm. However, these films may suffer from high pinhole densities and/or weak spots as observed from the occurrence of large number of extrinsic breakdowns below electric fields of 6 MV/cm.

The influence of PMA in different ambients on the electrical properties of silicon nitride films were examined. Films were subjected to N_2 anneal, forming gas anneal, and both N_2 and forming gas anneal at 420 ^{0}C. The electrical properties of silicon nitride films deposited after the formation of a thin (~4 nm) plasma deposited silicon oxide as the interface are also studied. Silicon nitride films subjected to both N_2 and forming gas anneal were found to have superior electrical properties to those of films annealed in either N_2 or forming gas ambients alone. The net bulk and interface charge density, charge trap density, D_{it} in the mid-bandgap region, and leakage current through the films were all lower for films annealed in both N_2 and forming gas ambients compared to the values for films annealed in either N_2 or forming gas ambients alone. All films exhibited higher instability due to charge trapping under negative gate bias stressing than under positive gate bias stressing. Silicon nitride films deposited on a thin (~4 nm) plasma deposited oxide showed much less charge trapping than the films with

no oxide interface, though the former had higher net effective fixed charge and interface state densities. The higher barrier to hole injection at the silicon oxide-silicon interface might be responsible for lesser charge trapping observed in these nitride-oxide films. The lack of charge trapping under positive gate voltage conditions aided by the higher barrier to hole injection from the substrate resulted in these nitride-oxide films exhibiting no hysteresis-type instabilities. The higher flatband voltage values for nitride-oxide layers may be attributed to the presence of nitride-oxide interfacial charge.

Silicon oxynitride films were deposited by introducing N_2O gas into the disilane/ammonia/helium gas system. The flow rate ratio of NH_3 to N_2O was varied from 2 to 20 by varying the N_2O flow rate. Higher N_2O flow rates resulted in higher deposition rates for silicon oxynitride films. Also, films deposited using higher N_2O flow rates exhibited higher net effective fixed interface charge densities. This behavior is explained in terms of the presence of an interfacial layer that forms during the early stages of plasma deposition due to the lower molecular dissociation energies of disilane and nitrous oxide compared to that of ammonia. Support for this is derived from the higher flatband voltages exhibited by nitride-oxide films compared with nitride films of equivalent thickness. All oxynitride films investigated except the ones deposited at NH_3 to N_2O flow rate ratio of 2 showed interface trap densities comparable to that of silicon nitride films. The instability due to charge trapping in the oxynitride films was found to be less than in nitride films. The charge trapping in the films decreased with increasing N_2O flow rates employed in deposition except at the highest N_2O flow rate investigated. This was also found to be the case with the leakage current observed through these films. In general, a turn-around behavior was observed in the trend for several electrical

properties of the oxynitride films for N_2O flow rates beyond 5 sccm in the system used in this work, indicating the importance of identifying an optimum flow rate ratio of NH_3 to N_2O depending on the application of the films. Also, chemical analyses of the oxynitride films would have to be carried out to relate the various properties of these films to their atomic composition both in the bulk and at the interface. All the oxynitride films examined exhibited fewer occurrences of extrinsic breakdown compared to silicon nitride films, indicating reduction of pinhole density in the oxynitride films. This could be an important issue in TFT gate dielectric process where films are deposited over large substrate areas and very few defective pixels can be tolerated. In fact, over 90% of the samples investigated showed intrinsic breakdown fields of higher than 10 MV/cm. Reviewing the overall properties of these nitride and oxynitride films, it was deduced that the silicon oxynitride films deposited by incorporating a N_2O flow rate of 1 sccm into the optimized silicon nitride deposition process in this work (with ammonia flow rate of 20 sccm and disilane flow rate of 1 sccm) would be the most practical choice for their use as gate dielectric films in thin film transistor (TFT) applications.

In summary, disilane was used, for the first time, in extensive process characterization of PECVD of silicon nitride and oxynitride dielectric films. The electrical properties of these films, espeically oxynitride films, are seen to be compatible with what is required of gate dielectrics in TFT applications. This fact coupled with the potentially higher growth rates in the disilane system make these films a viable gate dielectric alternative in the active matrix LCD industry.

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APPENDIX

LETTERS OF PERMISSION

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Process characterization of plasma enhanced chemical vapor deposition of silicon nitride films with disilane as silicon source

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(Received 22 August 1997; accepted 6 February 1998)

Process characterization details are reported for the first time, to the best of our knowledge, for plasma enhanced chemical vapor deposition of silicon nitride films using disilane as silicon source. Respectable deposition rates have been realized even under the conditions of low mass flow rates of disilane (<1 sccm) and large dilution of process gases with helium. The film uniformity (<±3% thickness variation across 4 in. diameter wafers) and process repeatability in this gas system were found to be excellent. The deposition rates were examined as a function of gas flow ratio, rf power, process pressure, and deposition temperature. Similar to a silane based process, two regimes of operation, namely ammonia-rich and disilane-rich, were identified. Films deposited at the boundary of these two regimes were nitrogen rich and had deposition rates that were dependent only on disilane to ammonia flow ratio and rf power and nearly independent of process pressure and deposition temperature. The hydrogen concentration of these films was found to be nearly constant over the investigated range of ammonia to disilane flow ratio values varying from 4 to 20. Also, the variation in H concentration in these films with deposition temperature was smaller than what is reported for silane based films. The choice for process parameters based on rf power, utilization of disilane, deposition rate, and film stoichiometry is given. © *1998 American Vacuum Society.* [S0734-211X(98)03703-2]

I. INTRODUCTION

Silicon nitride ($Si_xN_y:H_z$) films prepared by plasma enhanced chemical vapor deposition (PECVD) technique have received wide attention over many years as layers for insulation and passivation in device fabrication.[1,2] More recently, their use as gate insulators in ultralarge scale integration (ULSI) metal-insulator-semiconductor field effect transistors (MISFETs) and in thin film transistors (TFTs) deposited at low temperatures has continued to sustain research interest in these films.[3]

Plasma depositions are actually low pressure gas polymerization reactions where electron energy in the plasma is utilized to dissociate the precursor molecules to create highly reactive radicals that through gas phase and/or surface reactions produce the desired films. Currently, PECVD silicon nitride films are usually obtained by using silane (SiH_4) as the silicon source and either NH_3 or N_2 as the nitrogen source. Disilane (Si_2H_6) has been known to give better processing thermal budget for low temperature silicon[4] and SiO_2[5] film deposition. Recently Song *et al.*[6,7] have reported PECVD of SiO_2 films using Si_2H_6 as silicon source demonstrating better chemical and electrical properties of these films deposited at 120 °C than those of films deposited using silane or tetraethylorthosilicate (TEOS) at higher temperatures. Disilane requires lower activation energy[8] than silane and the two silyl radicals generated from plasma dissociation of disilane molecule have a large amount of excess energy making them highly reactive.[9] This situation is different from the decomposition of silane, where a large amount of the excess energy is shared by the H atom, but only a little by the silyl radical.[10]

In this article, we report, for the first time to our knowledge, the process details for the deposition of PECVD $Si_xN_y:H_z$ films in $Si_2H_6/NH_3/He$ gas system. Helium is used as the dilution gas with a flow that is two to three orders of magnitude higher than that of disilane. Although this results in reduced deposition rate, the benefits of dilution with helium, an inert and light gas, in terms of suppression of gas phase nucleation, better thickness uniformity of films deposited, and reduced plasma-induced damage of film-substrate interface are well known.[11] The characterization was carried out with the process gas flow ratio, process pressure, substrate temperature, and rf power as the process variables. Deposition rate, etch rate, refractive index, and bonding configuration in the films were examined as a function of different process parameters.

II. EXPERIMENT

The apparatus used for the film deposition, described elsewhere,[6] consists of a conventional parallel plate plasma reactor. Gases are supplied through a uniform array of holes in an 11 in. diameter upper electrode powered by rf at 13.56 MHz. The substrate is placed on the grounded bottom electrode. The substrate temperature can be controlled up to 300 °C by resistive heating. The upper electrode was always maintained at 60 °C. Boron doped, chemically polished 4 in. diameter 5–10 Ω cm Si wafers of (100) orientation were used as the substrates. After loading the wafers, the chamber was pumped down to a base pressure of 3×10^{-4} Torr. The process gases used were 5% Si_2H_6 in He base, 99.9995%

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VITA

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DOCTORAL EXAMINATION AND DISSERTATION REPORT

Candidate: Giridhar Nallapati

Major Field: Electrical Engineering

Title of Dissertation: Plasma Enhanced Chemical Vapor Deposition of Silicon Nitride and Oxynitride Films Using Disilane as Silicon Source

Approved:

P. K. Ajmera
Major Professor and Chairman

Dean of the Graduate School

EXAMINING COMMITTEE:

Date of Examination:

14 Dec 1998

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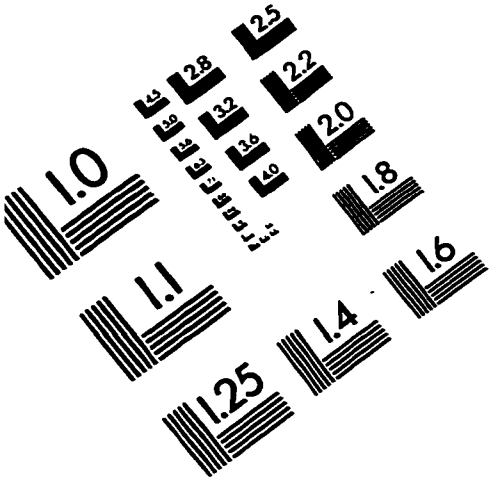

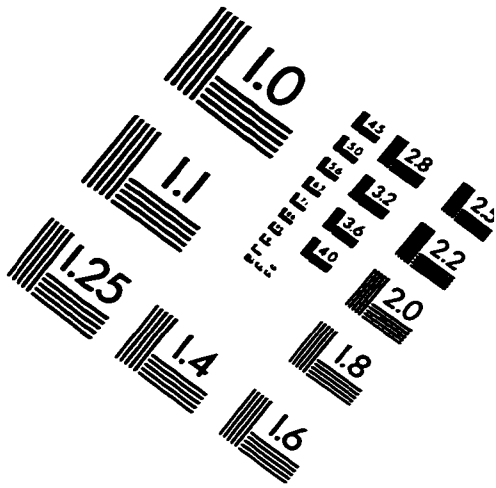

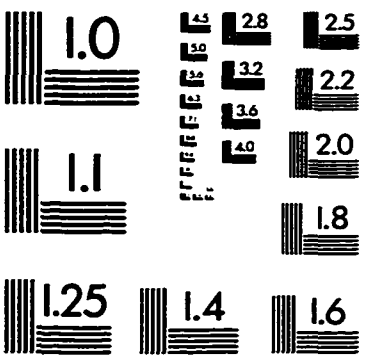

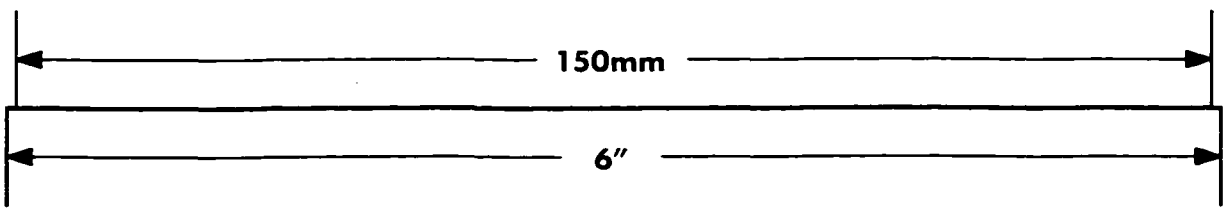

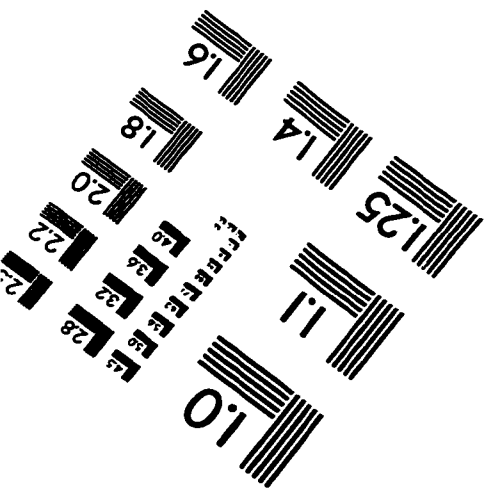

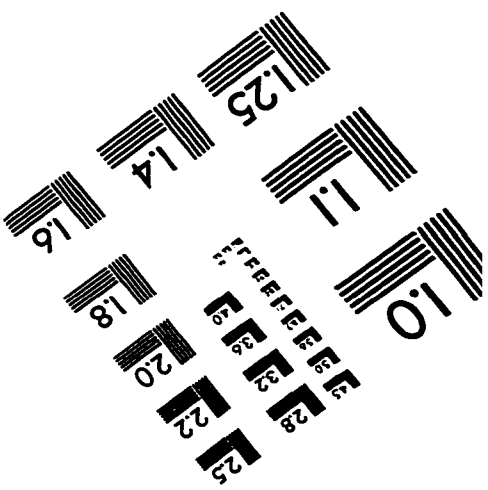

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